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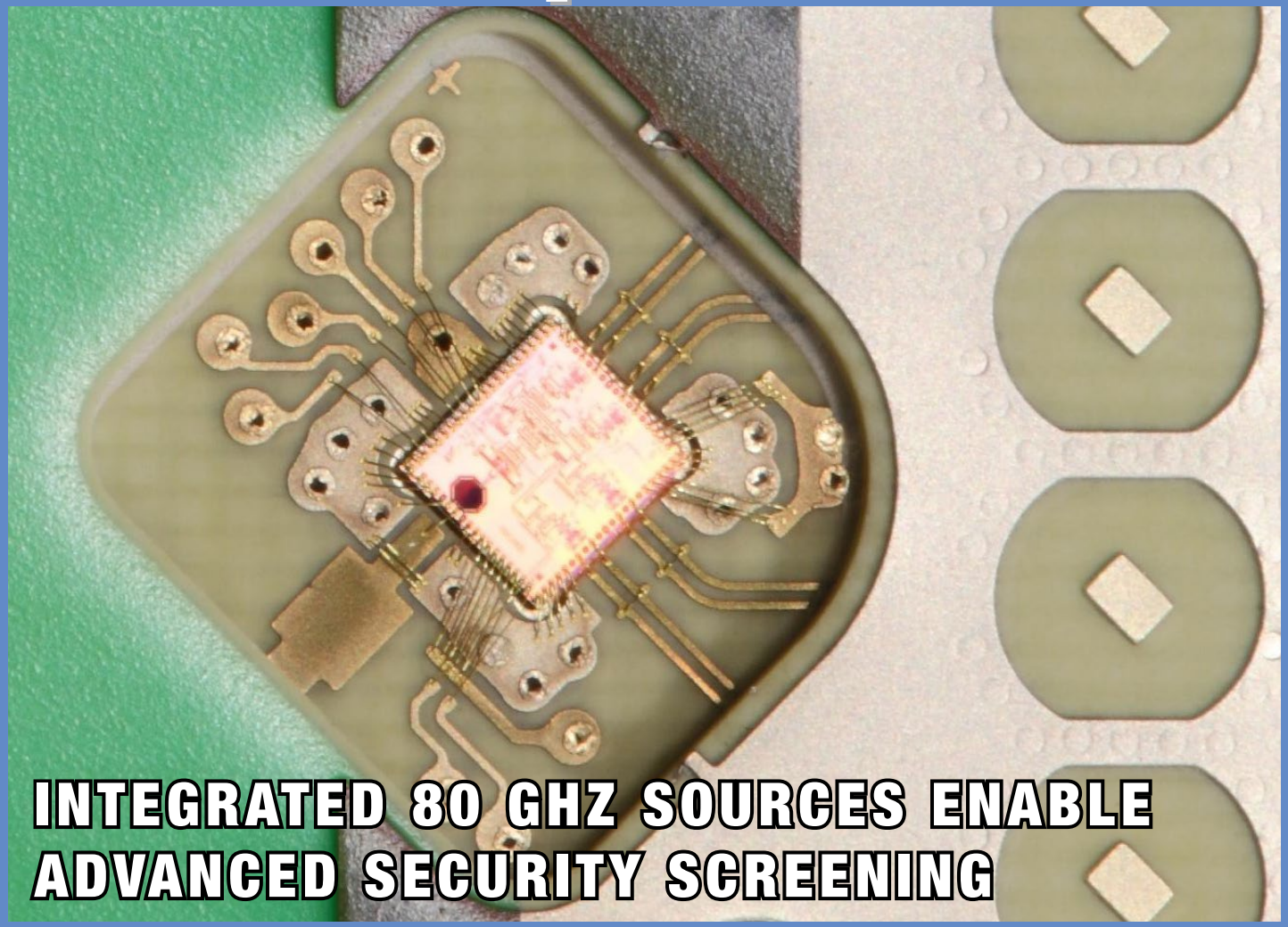

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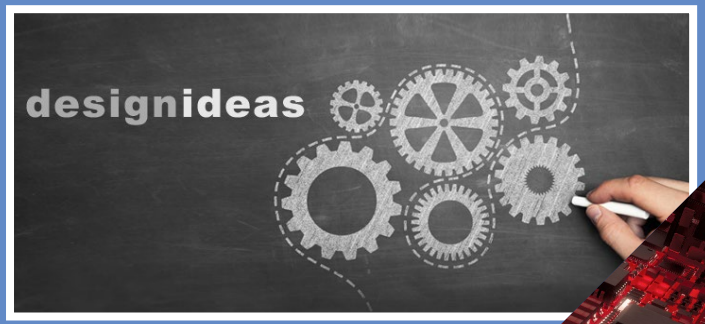

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COVER

Millimetre wave expertise enables faster, more efficient security screening

If you are travelling by air in the coming holiday season, you may find yourself being security scanned using mmWave techniques. Rohde & Schwarz – that readers of these pages usually know better as a test & measurement or RF communications provider – recently entered this market with a design that the company says represents a marked step forward from existing products in the security market. EDN Europe invited R & S to provide some insight as to how the company's RF and T&M experience has been applied to this use of mmWave technology. You can read more in the article on page 17

FEATUREARTICLES

ONLINE THIS MONTH

New Multiplier-Accumulator accelerates polynomials

New possibilities for smart-factory security

Understanding and designing differential filters for communications systems

EDN's columns

M&A, OR, LET'S BUY SOMETHING!

As 2016 comes to a close, there can be no doubt that one of the phenomena that has marked it out has been the seemingly endless stream of takeovers in the electronics industry. The activity is generically labelled M&A, mergers and acquisitions, but few of this year's deals have been in any real sense mergers. Straightforward acquisitions have been the predominant model.

The driving forces behind the trend are easy to identify; economies across the world are marking time, with limited opportunities for "organic" growth. There is no shortage of unemployed capital looking for something to do; money is cheap. Managements – not only in the semiconductor/electronics sector – are under shareholder pressure to improve results and if you can't readily grow the numbers by internal growth, then boosting turnover by a corporate transplant is an obvious option. For companies fortunate enough, or well-managed enough, to have their own cash reserves, these are not good times for the cash-at-bank line on the balance sheet. In an era of minimal or even negative interest rates, there is a need to get that money working.

There are too many such deals to revisit many of them them here; but they have touched the IP business (ARM to Softbank, July); semiconductors both integrated (NXP to Qualcomm, October) and fabless (Lattice to Chinese owners, November); and the distribution sector (Premier Farnell to Avnet, July).

Executing successful acquisitions is a very difficult process. Estimates vary, but when analysts pronounce on what proportion of large-company M&A exercises end up with a clearly positive outcome, the percentages are not high. Very early in the typical acquisition announcement, the term "synergy" will appear. Synergy is a word I try to avoid. If I do use it, I will intend the sense to be the potential for activities to combine harmoniously to yield an overall outcome that is more than the sum of the parts. One plus one yields more than two.

In the typical M&A press statement, "synergy" has come to mean the opportunities to eliminate overlap in corporate functions (which means people) to reduce the combined business' costs. Which leads directly to one of the classic M&A problems; you embark on a path that is intended to be about adding and growing, but your immediate focus and mindset has to be on cutting and shrinking.

The hazards of the M&A process are many, far too many to work through here. But 2016's crop of deals has demonstrated most of them. At the most basic level, for staff of the acquired and acquiring companies, is the question, "Do I still have a job?" And, "if I do, am I going to enjoy working here any longer?" For example, I have rarely heard executives of an acquired company so openly apprehensive as in one interview I conducted this year, "We have always had a simple management structure, only three layers: they [the acquiring company] have at least twice that. How is that going to work?"

From such seemingly minor concerns, much heartache can flow.

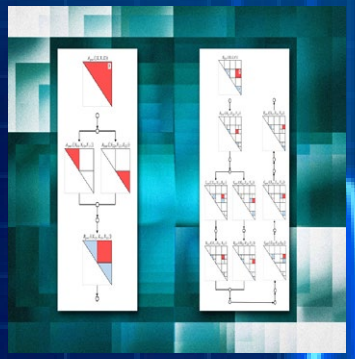
On the customer side – that's you, reading this column – there is the worry, "Will the product line that my project depends on, be a casualty of this merger? Even if it's still on the combined company's catalogue, will it have the same level of support?" Thus – again, just one example – the electronica trade show saw Microchip (bought Atmel, January) energetically broadcasting the message, "Yes! We definitely are going forward with both microcontroller architectures [PIC and AVR]"

Part of the organic process that has shaped the industry we know, is exactly the fact that some of these deals work out, and some don't. Occasionally you can look back at the outcome of such a merger and see a dynamic entity expanding into new territory that its constituent parts might not have reached. But perhaps not often. Product lines, technologies, divisions and most importantly, people, will be scattered to new homes as part of the continuing fall-out.

And – to close on a more positive note – some of those will be part of the next crop of technology innovators.

graham.prophet@eetimes.be

pulse

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Microsemi
SoC FPGA


wireless BMS
SmartMesh
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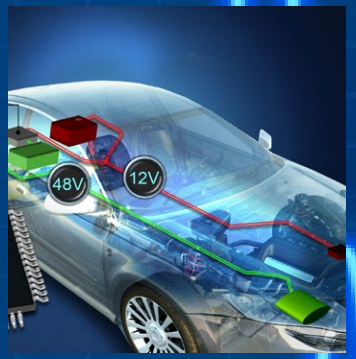
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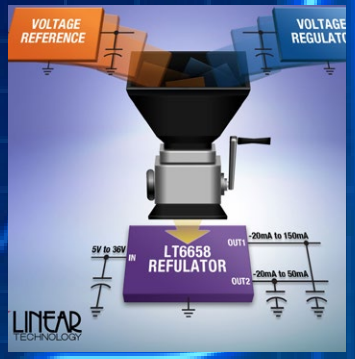
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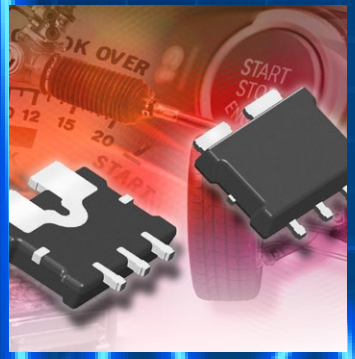
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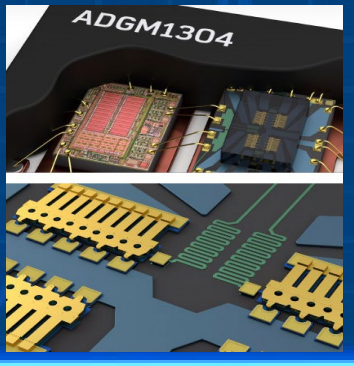
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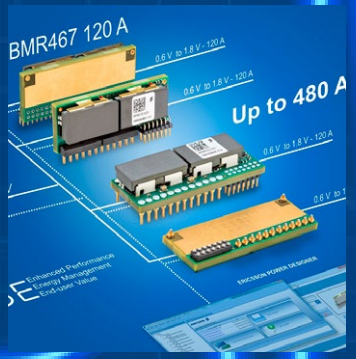
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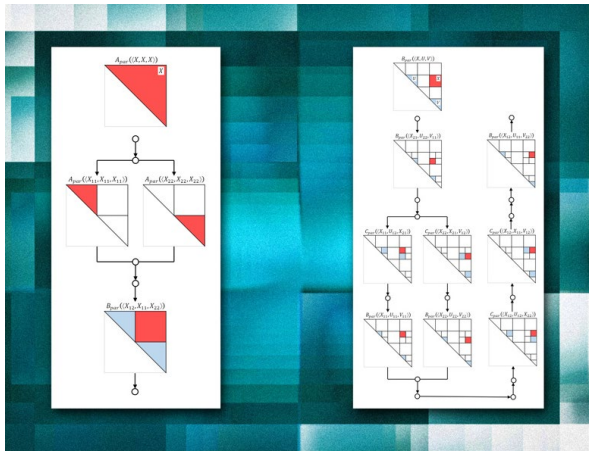
Automatic parallelisation research promises faster code by non-experts

Researchers at MIT have reported work that they say will allow non-specialists – that is, not specialised in the process of manually coding parallel execution of program flow – to optimize programs that run on, and make best use of, multiprocessor chips.

Dynamic programming – says the MIT information release – is a technique that can yield relatively efficient solutions to computational problems in economics, genomic analysis, and other fields. But adapting it to computer chips with multiple cores requires a level of programming expertise that few (for example) economists and biologists have.

In experiments, the researchers used the system to "parallelize" several algorithms that used dynamic programming, splitting them up so that they would run on multicore chips. The resulting programs were between three and 11 times as fast as those produced by earlier techniques for automatic parallelization, and they were generally as efficient as those that were hand-parallelized by computer scientists.

Dynamic programming offers exponential speedups on a certain class of problems because it stores and reuses the results of computations, rather than recomputing them every time they're required.



"But you need more memory, because you store the results of intermediate computations," says Shachar Itzhaky, first author on the new paper and a postdoc in the group of Armando Solar-Lezama, an associate professor of electrical engineering and computer science at MIT. "When you come to implement it, you realize that you don't get as much speedup as you thought you would, because the memory is slow. When you store and fetch, of course, it's still faster than redoing the computation, but it's not as fast as it could have been."

Computer scientists avoid this problem by reordering computations so that those requiring a particular stored value are executed in sequence, minimizing the number of times that the value has to be recalled from memory. That's relatively easy to do with a single-core computer, but with multicore computers, when multiple cores are sharing data stored at multiple locations, memory management become much more complex. A hand-optimized, parallel version of a dynamic-programming algorithm is typically 10 times as long as the single-core version, and the individual lines of code are also more complex.

The CSAIL researchers' new system — dubbed Bellmania, after Richard Bellman, the applied mathematician who pioneered dynamic programming — adopts a parallelization strategy called recursive divide-and-conquer. Suppose that the task of a parallel algorithm is to perform a sequence of computations on a matrix. Its first task might be to divide the matrix into four parts, each to be processed separately. But then it might divide each of those four parts into four parts, and each of those into another four parts, and so on. Because this approach — recursion — involves breaking a problem into smaller subproblems, it naturally lends itself to parallelization.

With Bellmania, the user simply has to describe the first step of the process — the division of the matrix and the procedures to be applied to the resulting segments. Bellmania then determines how to continue subdividing the problem so as to use memory efficiently.

Complete article, here

3rd-generation silicon carbide tech in FETs, SBDs and modules

Rohm Semiconductor is now fabricating devices in a 3rd generation of SiC technology, for MOSFETs, SiC Schottky Barrier Diodes (SBDs) and SiC modules. Rohm says it is now mass-producing the first trench-type SiC MOSFETs. This generation of SiC MOSFETs reduces on-resistance by 50% across the entire temperature range and input capacitance by 35% in the same chip size compared with planar gate-type SiC MOSFETs. This also makes it possible to reduce the size of peripheral components such as coils and capacitors by increasing switching frequency. The new SCT3080KL 1200V SiC MOSFET series in a TO-247 package is an example. 650V FETs in that package are available with 120 mΩ down to 17 mΩ on-resistance; at 1200V the range spans 160 to 22 mΩ. Rohm will also offer an AECQ qualified SiC MOSFET based on its 2nd Gen planar series.

The 3rd generation of SiC Schottky Barrier Diodes (SBD) realise lowest forward voltage (VF) and lowest reverse leakage current (IR) over the entire temperature range among all of the SiC SBDs currently available, Rohm claims. In addition to this, they feature high surge current capability for power supply applications. Adding to the recently announced TO220AC devices at 650V/6, 8 and 10A, Rohm has introduced D2PAK and TO220FM devices also adding lower current options, 2A and 4A to the family. Full SiC modules include chopper type modules for converters and integrate both trench SiC MOSFETs and SiC SBDs. In addition to 2 in 1 type modules, 1200V/120A,180A and 300A Chopper type modules are being prepared. Rohm adds that it is working on a new power module which will exhibit lower stray inductance.

Complete article, here

Microsemi offers open RISC-V core, in FPGA, for embedded designs

Microsemi has announced that its FPGA devices can be configured with a processor core in the Open RISC-V Architecture: the offering comprises an IP core and comprehensive software solution for embedded designs and will be implemented on IGLOO2, SmartFusion2 and RTG4 devices. Microsemi says it is the first field programmable gate array (FPGA) provider to offer a comprehensive software tool chain and intellectual property (IP) core for RISC-V designs. The company's RV32IM RISC-V core is available for Microsemi's IGLOO2 FPGAs, SmartFusion2 system-on-chip (SoC) FPGAs or RTG4 (radiation-tolerant) FPGAs, with an Eclipse-based SoftConsole integrated development environment (IDE) hosted on a Linux platform and the Libero SoC Design Suite providing full design support.

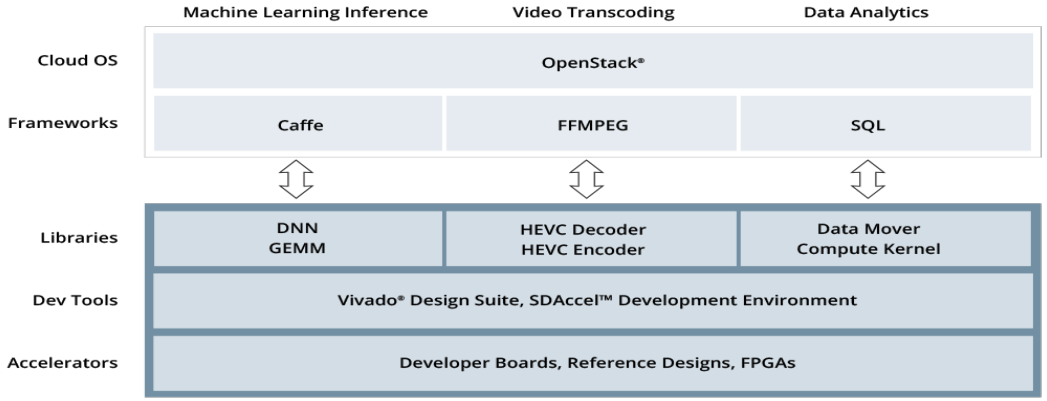
Microsemi's RV32IM RISC-V core, developed in collaboration with SiFive, enables engineers to design with an open instruction set architecture (ISA), enabling complete portability and a more secure pro-

cessor architecture governed by a permissive BSD license. RISC-V is an ISA which is now a standard open architecture under the governance of the RISC-V Foundation. RISC-V offers, Microsemi says, a 'compelling' soft processor solution for low power, reliable, secure FPGAs, "Now engineers can rely on an open ISA, without being tied to a single vendor and make use of open source tools and hardware. Never before has a processor allowed designers to inspect, modify, adapt, collaborate and migrate their design to the best platform for their product." The Libero SoC Design Suite is ready to implement the IP and, Microsemi adds, will efficiently pack [the core into] the FPGA logic elements (LEs), yielding a cost-effective solution. The Eclipse-based SoftConsole IDE running on Linux allows users to compile and debug their source code. For applications such as safety and security, the register transfer level (RTL) source code is available for inspection; customers can verify the security of the processor themselves, which is not possible with other processors, as they have closed architectures. In safety-critical applications, as customers can run multiple RISC-V cores to ensure if one fails, there is a redundant core to take over.

Complete article, here

Xilinx dynamic reconfiguration offers compute efficiency gains

Intended to accelerate mainstream adoption of Xilinx FPGAs in hyperscale data centres, the company has disclosed technology designed to enable the world's largest cloud service providers (and offered, at present, only to them) to rapidly develop and deploy acceleration platforms. Designed for cloud scale applications, the FPGA-powered Xilinx Reconfigurable Acceleration Stack includes libraries, framework integrations, developer boards, and OpenStack support. It provides the fastest path to realize 40x better compute efficiency with Xilinx FPGAs compared to x86 server CPUs and up to six times the compute efficiency over competitive FPGAs. Using dynamic reconfiguration, Xilinx enables silicon optimization for the broadest set of performance-demanding workloads including machine learning, data analytics, and video transcoding. These workload optimizations can be done in milliseconds by swapping in the most optimal design bitstream. Xilinx attributes the 2-6x gain in compute efficiency in machine learning inference to DSP architectural advantages for limited precision data types, and greater on-chip memory resources.



Xilinx Reconfigurable Acceleration Stack

The Xilinx Reconfigurable Acceleration Stack includes math libraries designed for cloud computing workloads, application libraries integrated with major frameworks, such as Caffe for machine learning, a PCIe-based development board and reference design for high density servers, and an OpenStack support package making Xilinx FPGA-based accelerators easy to provision and manage.

Complete article, here

Cortex-M4 ultra-low-power MCUs for wearables, from Maxim

Maxim configured the MAX32630 and MAX32631 ARM Cortex-M4F-based microcontrollers to provide fast processing in a tiny package, while extending battery life, for designs including high-performance fitness and medical/wearable devices.

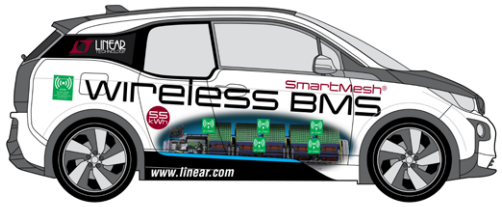
The MCUs' power management maximizes run time and provides the lowest energy consumption, in active (127 µW/MHz), DMA (32 µW/MHz), and retention sleep (3.5 µW) modes. The microcontrollers offer ample onboard code (2 MB flash), data (512 kB SRAM), and cache (8 kB) memory, to run third-party applications and logging sensor data. Interfaces include SPI, SPI XIP, UART, I²C, 1-Wire, and USB ports. Peripheral functions include six 32-bit timers, clock, 66 general-purpose I/O pins, pulse train engine, and 10-bit analogue/digital converter (7.8 ksamples/sec) The MAX32631 adds a trust protection unit (TPU) that enables advanced hardware encryption and authentication features, providing customers with a complete security toolbox to protect IP, algorithms, and user data. The MAX32630 and secure MAX32631 are based on the Cortex-M4F 32-bit microcontroller core with floating-point unit, and are packaged in a 4.37 × 4.37 mm 100-ball WLP package. An evaluation kit is available: MAX32630-EVKIT, with pricing starting at $150.00. MAX32630 pricing starts at $6.66 (1000).

Complete article, here

Linear Technology demos electric-vehicle wireless battery management

At the electronica 2016 exhibition, Linear Technology featured a BMW i3 'concept car' in which the internal communications between battery management PCBs within the main traction battery pack are implemented by wireless links, using its own Dust Networks 2.4 GHz mesh networking.

The wireless BMS concept car, developed by Linear's design partner LION Smart, combines Linear's highly accurate battery stack monitors with its SmartMesh wireless mesh networking, replacing the conventional wired connections between the battery packs and the battery management system. Benefits, Linear says, include the potential for improved reliability, lower cost and weight, and reduced wiring complexity for large multicell battery stacks for electric and hybrid/electric vehicles.



The demonstration also uses battery packs from Kreisel Electric, specialists in maximising the performance of 18650 cylindrical cells; the company builds battery packs that are liquid cooled, and heated, with a system integrated with the car's HVAC system. Optimum charging, the collaborating companies explain, can only take place when the battery pack is at a constant 30C, and heating as well as cooling may be required. The partners claim that given sufficient available power, charging to 80% in 18 minutes is feasible.

Linear presents its high voltage battery stack monitors as offering leading accuracy and reliability, enabling battery management systems that maximize battery pack performance and longevity. The LTC6811 is a complete battery measuring device for hybrid/electric vehicles that can measure up to 12 series-connected bat-

tery cell voltages with better than 0.04% accuracy. Combining the LTC6811 with Linear's SmartMesh wireless mesh networking system addresses concerns associated with automotive wiring harnesses and connectors.
The wireless BMS concept car, Linear says, shows the promise of wireless technology to significantly improve reliability and simplify the design of automotive battery management systems.

Complete article, here

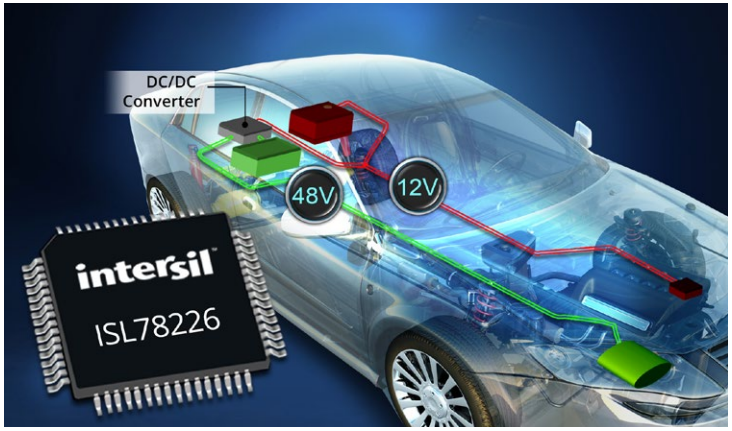
Wolfspeed offers free access to RF Tutorial series

Wolfspeed, supplier of gallium nitride on silicon carbide (GaN-on-SiC) high electron mobility transistors (HEMTs) and monolithic microwave integrated circuits (MMICs), is sponsoring one year of free access to a comprehensive multimedia engineering tutorial on passive and active RF circuits, including amplifiers. Entitled **"Conquer Radio Frequency: A Multimedia Conceptual Guide to RF & Microwave Engineering, Based on AWR Microwave Office Video Tutorials,"** the tutorial was written by Dr. Francesco Fornetti, a noted expert in advanced semiconductor materials and devices, including GaN HEMTs.
The online tutorial provides users with a full-colour reference textbook that serves as an introduction to the fundamental principles of both passive and active RF and microwave circuit design. In the more than 12 hours of circuit design video tutorials that accompany the textbook, Dr. Fornetti illustrates how to design, test, and characterize RF power amplifiers using the proprietary large signal GaN HEMT models that Wolfspeed developed for the NI (National Instruments) AWR Design Environment Microwave Office suite of design tools.

Complete article, here

12-48V, 6-phase, bidirectional DC/DC controller for dual-rail automotive

Intersil's ISL78226 is a bi-directional power conversion controller that is designed for 12V to 48V interconnection in hybrid cars and other vehicles.
The device is a 6-phase synchronous PWM controller that performs buck and boost conversion between buses. A single controller can deliver up to 3.75 kW with conversion efficiency of greater than 95%, and can interleave in a modular master/slave architecture (up to four chips) to achieve higher powers. 48V is appearing in more designs, Intersil says; it is more effective at delivering power to the road, and offers better regenerative braking. Alternators – in fact a starter/generator – in mixed architectures will be at 48V, so generating the 12V rail is a buck operation. Many functions that are now mechanically or hydraulically driven will be electrified; for example, oil pumps and electric turbochargers.
The ISL78226 eliminates the complexity of earlier designs, Intersil says. It re-



sponds to changing load requirements by dropping phases and can handle abrupt load changes. It has a PMBus interface, and internal limp-home mode. The chip can remove much of the complexity associated with design of a 48V 'mild hybrid', Intersil adds. The device is AEC-Q100 Grade-1 qualified for -40 to +125C operation.

Complete article, here

Ubuntu Core 16 delivers foundation for secure IoT

Canonical – the company that is the commercial face of Ubuntu – has issued Ubuntu Core 16 for the Internet of Things (IoT), with regular and reliable security updates, and app stores for intelligent connected devices. Ubuntu Core is a tiny, transactional version of Ubuntu for IoT devices and large container deployments. It runs a new breed of super-secure, remotely upgradeable Linux app packages known as snaps.

Major features of the package include; snap confinement ensures applications are trusted only with necessary data; the code meets industry and regulatory requirements for updates, operations and security; and provides mechanisms for ISV, manufacturer and enterprise control of updates.

The Ubuntu Core promises 'groundbreaking' security, management, operations and upgradability in a compact, developer-friendly platform, thanks to its use of 'snap' packages. Snaps are securely confined, read-only, tamper-proof application images, digitally signed to the integrity of IoT software. Update Control allows software publishers and manufacturers to validate updates across the ecosystem before they are applied. Snap updates are transactional, which means that failures are automatically rolled back, giving developers the confidence to update their applications regularly.

The operating system and kernel in Ubuntu Core are also delivered as snaps, so the entire platform is transactionally upgradeable.

All Ubuntu Core devices, from all manufacturers, will have free, regular and reliable OS security updates. "Ubuntu Core secures the Internet of Things and provides an app store for every device," said Mark Shuttleworth, founder of Ubuntu and Canonical.

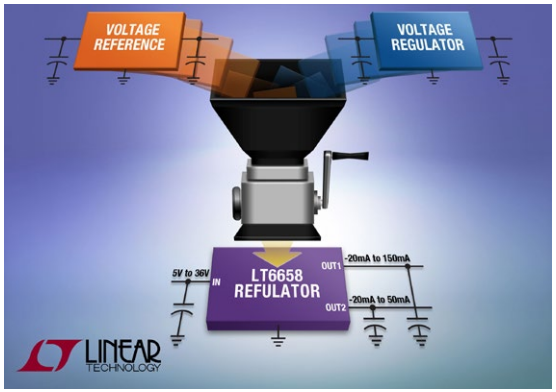
The universal or device-specific snap app store supports developers throughout the device lifecycle from beta testing to general availability, allowing them to sell IoT software as easily as cloud, enterprise and mobile software. A white label app store helps device manufacturers build a branded, differentiated device and software experience.

Complete article, here

Precision voltage reference drives up to 200mA, stable vs load

Linear Technology is calling its latest IC a "refulator" as it combines the functions of voltage reference and voltage regulator; LT6658 is a precision voltage reference that incorporates two high current output buffers. Based on a 2.5V bandgap voltage reference, each output can be separately configured for any voltage between 2.5V and 6V. Both outputs offer 0.05% initial accuracy, 10ppm/°C temperature drift and 1.5ppm of low frequency noise.

The device's outputs can drive up to 50 mA and 150 mA, respectively, and sink up to 20 mA. Typical load regulation is 0.1ppm/mA with up to 150 mA of load current. In parallel, the buffer outputs can be combined for even higher current capability. LT6658 is suitable for driving the reference input for a high resolution ADC or DAC using one output, while simultaneously supplying power to other devices using the second output. Both outputs track each other over temperature and

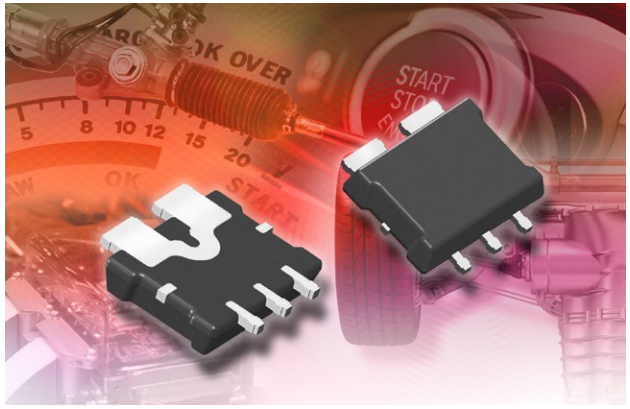


load, allowing them to address applications requiring ratiometric supply rails. The outputs have excellent supply rejection and are stable with up to 50 µF over the entire specified operating range. With this output capability, the LT6658 can serve as both reference and regulator combined. Alternatively, the LT6658 can be used to generate a reference plus a virtual ground, or as two matched, tracking references.

Complete article, here

100A, small-package current sensor ICs, with precision programming

Allegro MicroSystems' ACS780/ACS781 are fully integrated current sensor linear ICs in a core-less package designed to sense AC and DC currents up to 100A. This automotive-grade, low-profile (1.5 mm thick) sensor IC package represents the highest current density of any Allegro current sensor IC package to date. This package has a very small footprint and delivers extremely high power density for current sensing applications. The Hall sensor technology also incorporates common-mode field rejection to optimise performance in the presence of interfering magnetic fields generated by nearby current-carrying conductors.



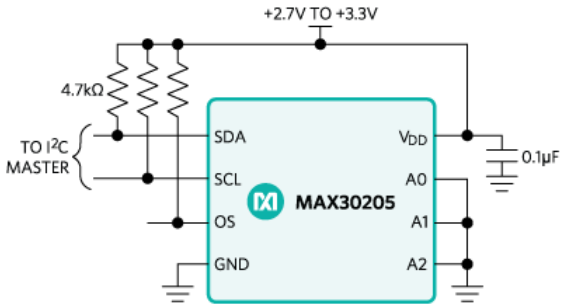
The devices consist of a precision, low-offset linear Hall circuit with a copper conduction path located near the die. Chopper-stabilized signal path and digital temperature compensation technology also contribute to the stability of the devices across the operating temperature range. High-level immunity to current conductor dV/dt and stray electric fields is offered by Allegro's integrated shield technology, for low-output voltage ripple and low-offset drift in high-side, high-voltage applications. The internal resistance of this conductive path is typically 200 µΩ, providing low power loss. The thickness of the copper conductor allows survival of the devices at high overcurrent conditions. The terminals of the conductive path are electrically isolated from the signal leads allowing the device to operate safely with voltages up to 100V peak on the primary conductor.

These sensor ICs are suited for automotive, industrial and computer applications. Automotive applications include EPS and DC/DC converters and oil and HVAC pumps that require higher currents. Industrial applications include low side sensing in VFD and other motor control systems.

Complete article, here

Clinical-grade human body temperature sensor has ±0.1°C accuracy

Maxim Integrated has posted details of the MAX30205 temperature sensor for thermometer applications. The sensor accurately measures temperature and provides an overtemperature alarm/interrupt/shutdown output. The chip converts the temperature measurements to digital form using a high-resolution, sigma-delta, ADC. Accuracy meets clinical thermometry specification of the ASTM E1112 when soldered on the final PCB. Communication is through an I²C-compatible 2-wire serial interface that accepts standard write byte, read byte, send byte, and receive byte commands to read the temperature data and configure the behaviour of the open-drain over-temperature shutdown output. The MAX30205 features three address select lines with a total of 32 available addresses. The sensor has a 2.7V to 3.3V supply voltage range, 600 µA supply current, and a lockup-protected I²C-compatible interface for wearable fitness and medical applications.



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Sigfox FCC-certified long-range RF transceiver from Microchip

Microchip claims the first FCC-certified – certified also for use in Europe – fully integrated RF transceiver and kits for developing IoT solutions for use on the Sigfox network; the ready-to-run package offers easy connectivity and low-power consumption for devices running on Sigfox's dedicated IoT network.

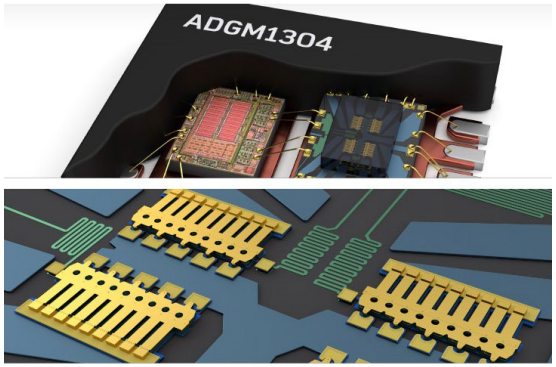
The ATA8520E transceiver is the first fully Sigfox-certified chip for North America and Europe and is supported by a standalone evaluation kit and Xplained PRO development boards. It hosts Microchip's highly integrated ATA8520E, a low-power RF transceiver with an integrated AVR microcontroller. The kits contain the first FCC-certified board that allows developers to connect to Sigfox's long-range, two-way global IoT network resulting in a low-cost, low-power device-to-cloud connectivity solution. The product is available in two versions. Customers can either purchase Microchip's Sigfox-certified ATA8520-EK as a standalone kit, designed primarily to test the technology, or as a kit combined with an Xplained PRO board for system-design purposes. Both are dedicated for Sigfox's IoT network in the licence-free ISM bands. The solutions come complete with the Sigfox library, modulation, ID and PAC code, and a security key enabling IoT developers to help get their design to market. Sigfox is currently operating in 24 countries and registering over 8 million devices in its network.

Complete article, here

MEMS-based RF switches now a 'commercial reality' says ADI

Analog Devices has introduced RF switch technology capable of 14 GHz operation, using chip-scale switching elements – MEMS switches – that it is initially aiming at markets such as test & measurement, to replace electromechanical relays. This will, ADI says, enable next-generation instrumentation equipment with increased channel density and extended speed, operating lifetime and reduced power consumption.

The first in a new product series, ADI's ADGM1304 and ADGM1004 RF MEMS switches are presented as 95% smaller, 30 times faster, 10 times more reliable, and use 10 times less power than conventional electromechanical relays. Future products within the MEMS switch series will replace relays in aerospace and defence, healthcare, and communications infrastructure equipment, allowing OEMs in those markets to pass similar size, power and cost savings along to their customers.



Unlike other switch alternatives such as solid-state relays, the ADGM1304 and ADGM1004 MEMS switches have superior precision and RF performance from 0 Hz (DC) to 14 GHz. ADI's MEMS switch solution contains two dice to maximize operational performance – an electrostatically actuated switch in a hermetically sealed silicon cap, and a low-voltage, low-current driver IC. The switching element has a highly conditioned, extremely reliable metal-to-metal contact that is actuated via an electrostatic force generated by the companion driver IC. The resultant co-packaged solution ensures best-in-class DC precision and RF performance, and makes the switch easy to use.

Complete article, here

Dialog backs Energous for free space wireless charging

by Nick Flaherty

Dialog Semiconductor is backing a new entrant to wireless charging with a $10m investment. Energous is the developer of WattUp, a new wireless charging technology that provides over-the-air power at a distance. Alongside the $10m investment in Energous, Dialog will be the exclusive component supplier of the WattUp chips while Energous use Dialog's sales and distribution channels.

WattUp uses RF frequencies to send power in a similar way to a Wi-Fi router and technology from startup Radient Micro-tech, and is a director of the AirFuel Alliance, which competes with the WirelessPower Consortium (WPC) that develops the Qi technology. The company raised $20m earlier this year.

Like Radient, WattUp differs from inductive or resonant wireless charging systems in that it delivers power at a distance, to multiple devices, in any orientation, resulting in wire-free charging. It uses Dialog's SmartBond Bluetooth low energy solution as the out-of-band communications channel between the wireless transmitter and receiver and Dialog's power management technology is then used to distribute power from the WattUp receiver IC to the rest of the device while Dialog's AC/DC Rapid Charge power conversion technology delivers power to the wireless transmitter.

WattUp uses small form factor antennas that are formed using the existing device's printed circuit board, removing the need for

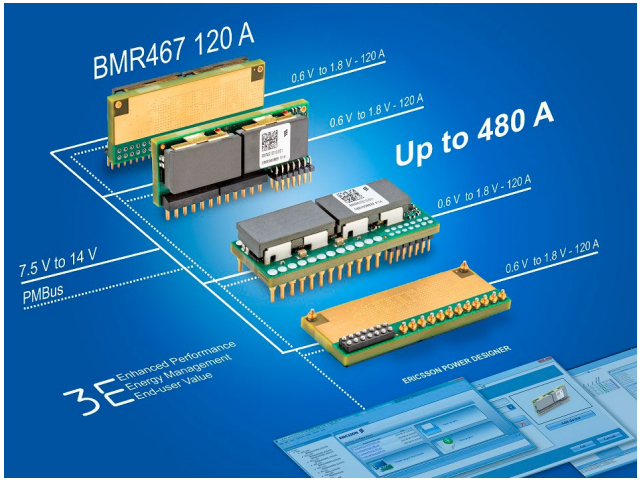
larger, more expensive coils used in competing solutions today. This enables broader adoption of wireless charging in a larger range of battery-powered devices, such as smartphones, tablets, Internet of Things (IoT) devices, small form factor wearables, and Virtual Reality (VR)/Augmented Reality (AR) devices. Energous hopes to tap Dialog's existing cutomers to grow the business.

Complete article, here

120A dual-phase DC/DC parallels up to 480A output

Ericsson Power Modules' BMR467 is a two-phase 120A fully digital point-of-load (POL) DC/DC power module that, with four devices operating in parallel, can deliver a total of 480A, representing a power density of 15 A/cm³ (250 A/in³); its SIP package format measures 50.8 x 19.05 x 8.2 mm.

The converter's features include Automatic Digital Compensation and a half-load efficiency of 93.2% at 12 Vin, 1.8 Vout. Delivering 30A per module more than its pin-compatible predecessor BMR465, the BMR467 is also compliant with the new 'teraAMP' AMP (Architects of Modern Power) specification.



Ericsson's design is fully digital, that is, the internal control loop of the converter is digital, which, among other benefits, Ericsson says delvers an efficiency curve that is flatter, and maximised, over more of its load range. The unit is ready for future Software-Defined Power Architecture (SDPA) systems, anticipated as a path to efficient and energy-optimized network architectures by 2020.

The BMR467 POL converter can be operated as a standalone unit delivering 120A at output voltages from 0.6V to1.8V, an output power up to 216W, as well as being part of a larger power system when processor boards require higher current. Built on a two-phase topology, the modules can become part of a multi-module and multiphase (up to eight-phase) power system that enables phase spreading, which reduces peak current and also the number of capacitors required by end systems. The module can be configured with support available via the downloadable Ericsson Power Designer software tool.

Complete article, here

8-bit AVR MCUs gain PIC-style Core Independent Peripherals

Following its acquisition of Atmel, Microchip has announced a new generation of 8-bit tinyAVR MCUs. From its PIC series, Microchip has applied the concept of core independent peripherals, that can exchange data without waking the main processor core, and implemented it in the tinyAVRs.

With this launch, Microchip says that it is reiterating both its intention to continue full support and

development for both PIC and AVR architecture; and its focus on 8bit. 8bit MCUs continue to sell in ever-growing volumes, the company says, and remain an appropriate choice for very many simpler, especially real-time, tasks.
The new series is supported by the START package (that generates 'housekeeping' code in C and frees development time for application coding) for graphical configuration of embedded software; it integrates rich features with 4 kB or 8 kB Flash in low pin-count packages; its core independent peripherals include a peripheral touch controller; and has self-programming for firmware upgrades and power-down mode with SRAM retention.
Four new devices range from 14 to 24 pins and 4 kB or 8 kB of Flash and are the first tinyAVR microcontrollers to feature Core Independent Peripherals (CIPs). Microchip notes that Atmel had previously implemented a feature very similar to CIPs, in some of its larger MCUs – the Event system. With this series, it has effectively migrated that feature down to the smaller devices.
"This announcement is very important to Microchip as it represents the coming together of the two most powerful 8-bit MCU brands under one roof," said Steve Sanghi, CEO and Chairman of the Board of Microchip Technology Inc. "Customers love both PIC and AVR MCUs and Microchip is re-energising new product development to not only continue to support, but to grow the AVR portfolio."

Complete article, here

Programmable mixed-signal IC technology adds power switching, sequencing

Silego Technology has extended its GreenPAK programmable mixed-signal IC architecture with a device that functions as a completely configurable and very small power management IC, with functions including voltage monitoring, power sequencing, reset and integrated low-on-resistance power switching.

Silego intends the SLG46125 to be the first in a series of parts designed to create "Flexible Power Islands" (FPI). In products with complex, multi-rail power supplies – or even in designs with less complex needs – Silego believes that designers frequently need to create or retro-fit sections of the power distribution with specific characteristics, that may not be handled in a single central PMIC. In common with other Silego parts, the SLG46125 might be used from the outset in a design, or employed to apply a late design change. The device integrates dual 45 mΩ / 2A P-FET power switches.
Using FPIs, designers can divide their complex power system into some number of local power regions (or islands), each of which includes the power control, power sequencing and power regulation needed to support loads in the immediate vicinity. Silego believes this technique results in higher performance and a more efficient solution that can be flexibly tailored to the requirements of each individual system.

Complete article, here

AIRPORT SECURITY SCREENING WITH MILLIMETRE WAVES

By Dr. Sherif Sayed Ahmed, Rohde & Schwarz

Fully-automated personnel scanning using a multi-channel millimetre-wave array, with intelligent image-recognition algorithms that perform real-time analysis on raw data, can protect passengers' safety by identifying threats accurately and clearly, while also preserving travellers' privacy by eliminating any need to render images on-screen or store data.

Introduction: stepping up airport security

Airport authorities responsible for preventing attackers boarding planes need an alternative to the basic metal detector gates now widely used at entrances and boarding points. Screening is time-consuming and imprecise, as the systems cannot determine the nature or exact location of a perceived threat. Every alarm must be investigated further by a human operative, and many are found to be "false positives". Moreover, such equipment cannot detect non-metallic weapons such as explosives, in particular, which are a major concern for today's airline operators.

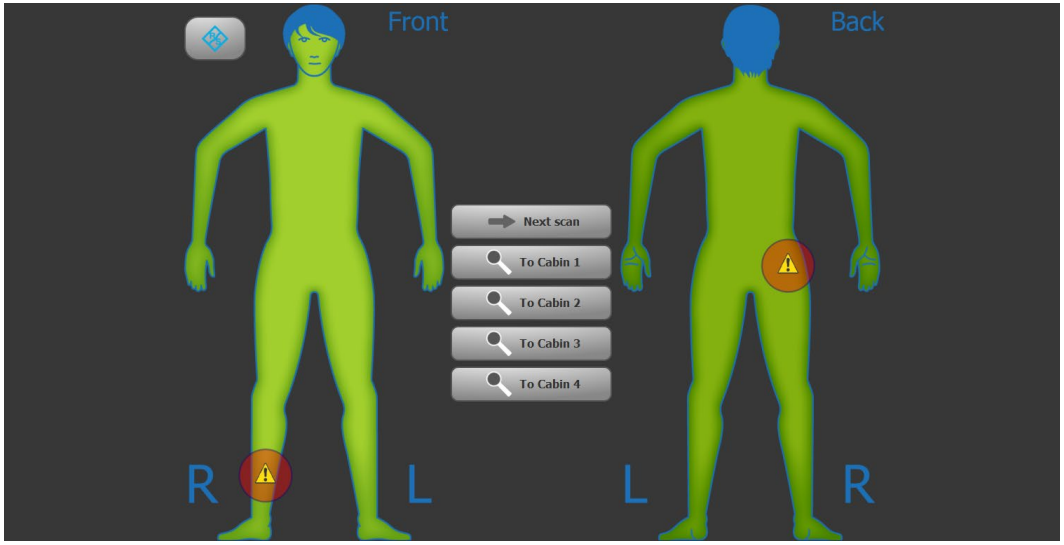


Figure 1. *When the R&S QPS security scanner reports an alarm, the location of the object is marked on an avatar, a symbolic graphic of the human body. No image of the scanned body is seen or stored.*

A fast and non-intrusive system is needed, which is able to "see through" clothes in order to detect concealed weapons or other proscribed items such as plastic explosives. Alternatives such as X-rays or ultrasound have a number of disadvantages: since X-rays have an ionising effect on body cells, some passengers – as well as security workers' representatives – may object to routine or repeated exposure. Ultrasound can only work at extremely close range using a coupling medium, such as a gel, which is obviously impractical in an airline scanning situation.

Scanning with millimetre waves offers an alternative. Some types of millimetre-wave scanners have already entered service in locations such as airports and public buildings. Unlike X-rays, millimetre waves have no ionising effect on organic tissue, and are not harmful to the human body. No physical contact with the body is needed to capture a 3D image, and the scan can be completed quickly to allow high throughput as is required in a busy airport scenario. However, some key challenges must be overcome.

Design to preserve privacy

Because millimetre waves do not penetrate the body, the image captured can present a detailed view of the surface of the body beneath clothing. Although this is ideal for de-

tecting almost any concealed object, including non-metallic weapons or explosive materials, there are obvious privacy concerns. Various initiatives have sought to address the issue: some authorities have introduced procedures to restrict the viewing and storage of captured images. However, the potential for breaches of such protocols to occur, or for misinformation about the handling of images to spread, could undermine confidence in the security systems that are intended to protect the travelling public. There is also the possibility for human error, when security staff are responsible for inspecting images individually at checkpoints, which may allow dangerous items to pass through.

Quick Personnel Security Scanner (R&S QPS) presents a technical solution to these challenges by completely automating the detection of concealed threats. No human-body images are presented on a screen for an operator to view, and no image data is stored. If a concealed object is detected, the system indicates its location on an avatar instead of displaying the passenger's own body (see Figure 1). Indicating the position of a suspect object in this way can help accelerate subsequent investigation, allowing harmless passengers to proceed quickly and those perceived as a threat to be detained confidently.

To achieve this, Rohde & Schwarz has introduced important new technologies with the QPS that permit cost-effective full-body scanning and signal processing at near real-time performance.

Technical choices

Several alternative approaches are viable for millimetre-wave imaging. Passive systems can be effective for outdoor use, where the background is cool relative to the scanned object. However, in an indoor environment there is less contrast between background and object temperatures. For this reason, a system designed for use inside an airport has to use active illumination whereby a millimetre-wave signal of very low power is emitted towards the person [subject], and receiving units analyse the resulting complex patterns. Known techniques for millimetre-wave imaging with active illumination utilise either mechanical scanning, which is unable to support the fast cycle times needed for high-speed airport-security systems, or dense monostatic antenna arrays that employ large numbers of antennas, resulting in prohibitive high system cost.

The R&S QPS uses a new approach that clusters and positions multiple transmit and receive antennas in a multistatic 2D array. Combined with digital beam-forming, these clusters create an electronically optimised aperture that allows a sparse and therefore low-cost antenna array to provide good image quality at close range. Close range imaging is optimal for human-body scanning due to the illumination limitations caused by the specular reflections out of the human skin at these frequencies. Thus long-range imaging is becoming impractical to find the small threats of interest.

In addition, the QPS is designed to operate at higher frequencies than conventional millimetre-wave systems. Operating in the 70-80 GHz frequency range allows higher signal bandwidth resulting in superior range resolution. Choosing this frequency range also allowed the development project to take advantage of design knowledge surrounding 77 GHz radar systems that is already established in the automotive industry.

In the continuation of this article, Dr Ahmed describes the antenna, signal generation and analysis chains that the test & measurement company created to address this alternative measurement domain – click for pdf.

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ADC INPUT IMPEDANCE MATCHING

BY IAN BEAVERS

The differential input to an ADC often originates as a single-ended signal from an antenna or other signal acquisition component. Before the signal can be delivered to the ADC, it must be converted to differential by an active device such as an amplifier, or a passive device such as a balun or transformer. In either case, the impedance matching within the path is critical to ensure that signal power is neither lost nor reflected back to the source.

First, it is important to understand the ADC's input impedance. Most high speed ADCs will have an input impedance of 50 Ω or 100 Ω, although other values are possible. The second factor is the output impedance of the device that drives the ADC. Ideally, the output impedance of this device should match the input impedance of the ADC, but this is not always possible. Third, the characteristic impedance of the transmission line between these components should match on both ends.

Sometimes, a passive input network is needed ahead of the ADC to create a matched termination impedance or to attenuate the signal. Care should be taken to calculate the discrete impedance values so the lumped equivalent network, when considering the ADC, matches the output impedance of the balun or amplifier. Passive component tolerances and parasitic effects should not be neglected as potential sources of imbalance.

While not an explicit component, matching the transmission line from the upstream signal source to the termination impedance at the ADC is equally critical. The characteristic impedance of the differential transmission line formed by the PCB traces must be maintained throughout, and must match the termination impedance. If the transmission line with Z0 is terminated into impedance less than Z0, there will be a reflection with opposite polarity back to the source. If the transmission line with Z0 is terminated into impedance greater than Z0, there will be a reflection with the same polarity back to the source.

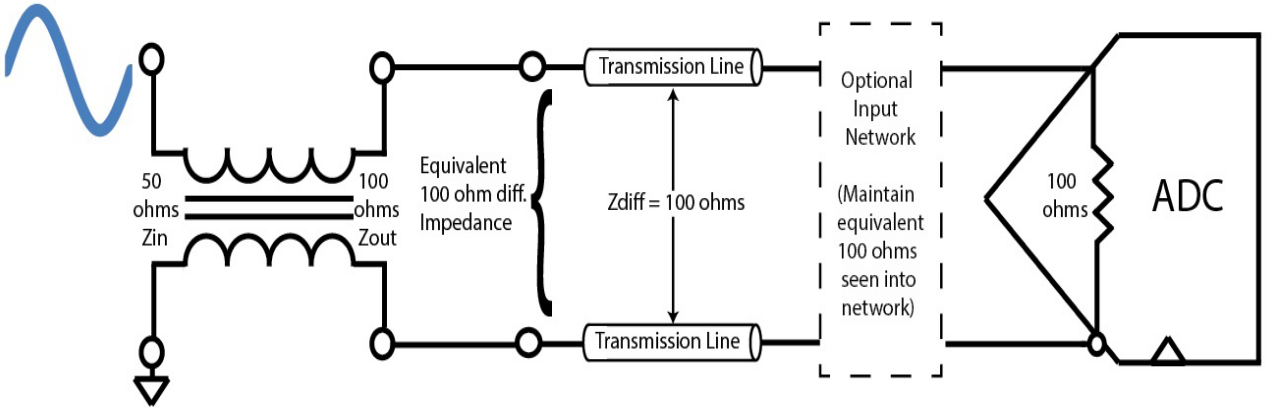

Figure 1. *Maintain a matched transmission line from the source to the ADC by carefully selecting the same impedance within active components and passive devices for any optional input network.*

In this example, a 100-Ω differential transmission line must match the 100-Ω ADC termination impedance and the 100 -Ω output impedance of the passive balun.

Ian Beavers [ian.beavers@analog.com], *a staff engineer for the Digital Video Processing Group at Analog Devices (Greensboro, NC), is a team leader for HDMI and other video interface products. With over 15 years' experience in the semiconductor industry, he has worked for ADI.*

OPTIMIZED FOR ADAS APPLICATIONS: NEW COMPILER CHALLENGES – PART 2

By Dr. Alexander Herz, Tasking

The compiler is a key tool for the cost-efficient design of ADAS applications. However, the tools currently available must be better adapted to this challenging task. This includes considering the code structures and specific safety requirements typical of ADAS applications.

When planning a compiler technology roadmap, you will inevitably touch the issue of advanced driver assistance systems (ADAS), which all major OEMs and software suppliers of the automotive industry are committed to. A closer look, though, will raise some questions: What requirements are placed on compilers and toolsets by ADAS applications? Are these things related at all? What are the differences between traditional automotive applications and ADAS applications?

In part 1 of this article, Dr. Herz looked at the challenges posed by ADAS applications; defining suitable architectures; code structures; and the problem of parallelisation. The article continues here; click the link below for a pdf of the complete article.

Hardware accelerator support

Intrinsics are the most straightforward method to support hardware accelerators. These constructs can be used to address special hardware instructions from C/C++. At the next level, special high-level languages, most of which are similar to C, are supplied enabling designers to address their hardware efficiently. Although these high-level languages require compilation and optimization, their closeness to the underlying hardware simplifies the whole process (OpenCL for NVIDIA, compiler from NVIDIA; C for GTM, compiler from TASKING; extended C for EVE from TI). As a final option, compilers can automatically detect code areas that can be executed efficiently by an accelerator in order to automatically generate the appropriate code (SIMD, icc). However, this fully automatic discovery is restricted in most cases because standard C/C++ code is not explicitly written for the specific accelerator. Quite often, minor code modifications yield excellent results, although a suitable tuning tool is indispensable in order to find and implement the necessary changes with reasonable overhead.

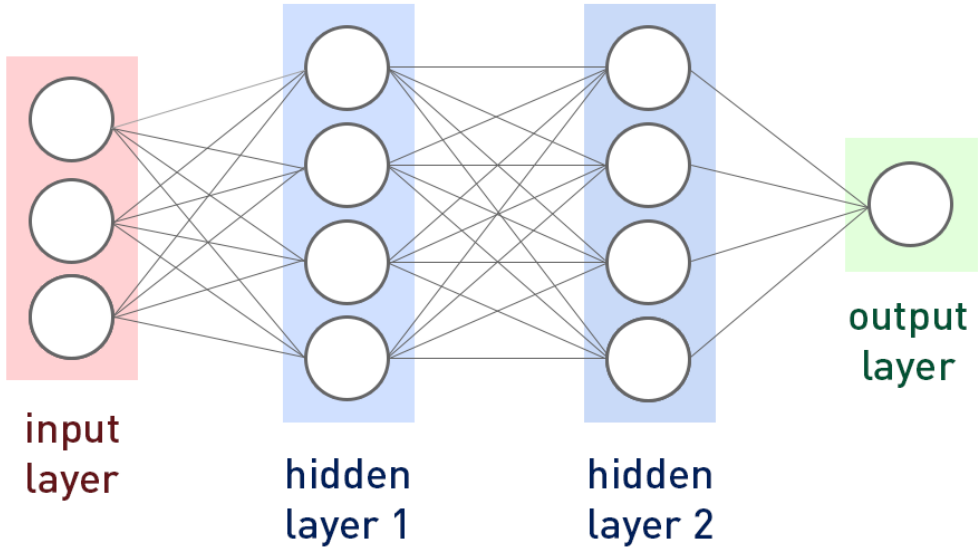

Figure 3. *Schematic diagram of a neural network*

Furthermore, many heterogeneous hardware architectures mandate that each programmable unit be addressed with its own compiler. In order to avoid dealing with an excessive number of incompatible tools, which would generate new safety risks, it is advisable to use tool environments that can address all programmable units and ensure mutual compatibility between the tools.

For instance, the TASKING tool environment for Aurix (Infineon) can be used to program and debug all units of the architecture from a single IDE. Interactions between units can be controlled and monitored more safely because symbol information is compatible between the different units.

Safety requirements for ADAS applications

In order to meet the specific safety requirements of ADAS applications, tools (modelling tools, compilers, analysis tools) and software components (OSs, libraries, etc.) relevant for these applications must be developed and qualified according to ISO 26262.

Some of the newer safety requirements can be understood using neural networks (Figure 3). Neural networks are software components that are often used for detecting and processing sensor data in ADAS applications. Although there are interesting prototypes based on neural networks, it is still not clear how a correct behaviour of these networks can be ensured in extreme situations.

At the moment, no known procedure can guarantee that neural networks always behave correctly without any risks for road users. Therefore, one cannot let neural networks make safety-critical decisions without a suitable supervisory entity. In addition to the hardware for the neural networks themselves, which will issue a hard-to-predict decision proposal based on the input data (e. g. accelerate to 100 km/h, pass on the left side, actuate an emergency stop, etc.), there must be a supervisory entity running on hardware featuring the highest safety certification (ASIL-D). The latter will operate using predictable algorithms to check if the proposal made by the neural networks can be executed safely or if a safer alternative should be chosen (Figure 4). For instance, the supervisory entity would check if the passing manoeuvre proposed by the neural networks can be executed without any risk. For this purpose, it will use its own, predictable calculations to check if there are no obstacles etc. Predictable algorithms are still being researched in some areas (e.g. data fusion) in order to create an effective supervisory entity.

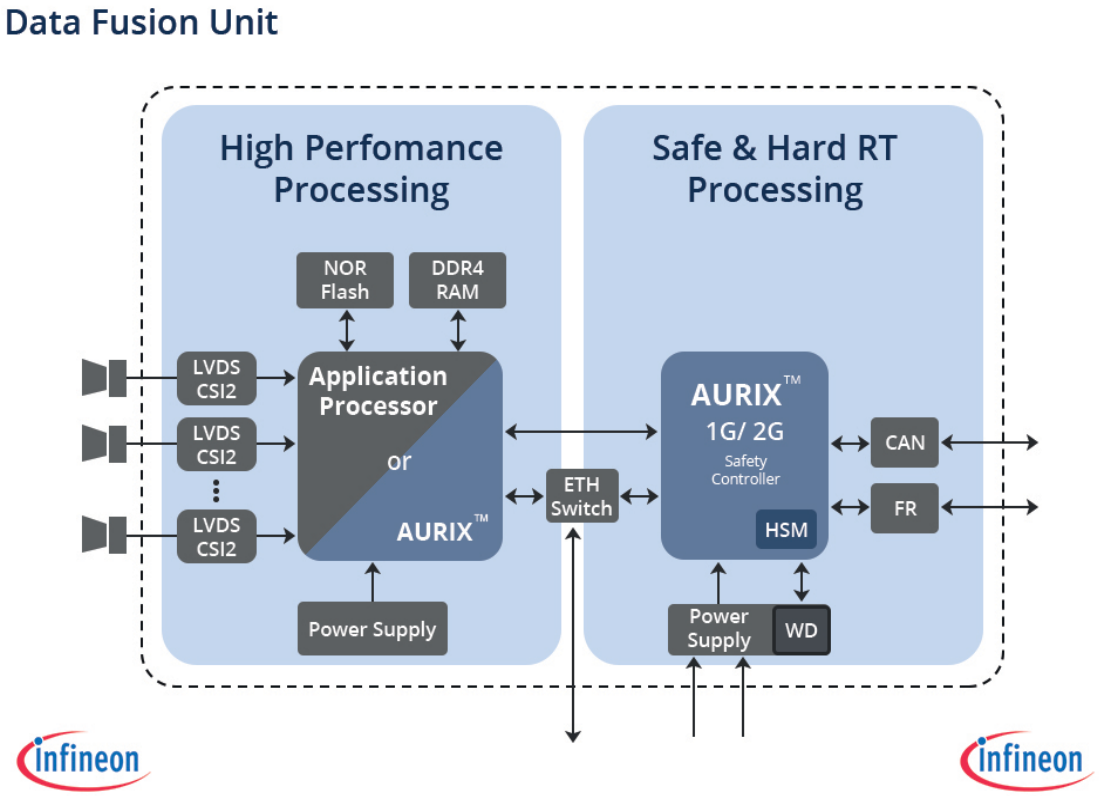

Figure 4. *High-performance processing for neural networks and image processing combined with safe processing for the supervisory entity*

Many of the predictable algorithms for ADAS applications are based on linear algebraic calculations supported by LAPACK and others. Optimized solutions including the LAPACK

Performance Libraries from TASKING can be used to implement these algorithms efficiently and safely on various target platforms.

The remaining parts of ADAS applications can be certified using several tools and processes that are helpful to meet various ISO 26262 requirements. Simple programming errors (including non-initialized data) can be detected efficiently using static analysis (Polyspace, Klocwork, etc.). For detection of safety relevant access violations (software components with different ASILs accessing each other and creating protection faults in the Memory Protection Unit – MPU), it is beneficial to use the TASKING compiler with its associated safety checker tool support. The compiler's integrated safety checker extension can be used to define different safety categories (e. g. ASIL A to D), to assign data and functions used in the project to different safety categories and to manage the access privileges between these categories.

This information can then be used for two purposes. First, the compiler is unable to perform certain optimizations (reverse inlining, code compaction) because these optimizations could result in safety access violations if they are performed without taking the access privileges into account. Second, the same information can be used with the TASKING safety checker tool (which can also be obtained for third party compilers, if desired) to identify undetected access violations that would generate MPU exceptions without any additional testing overhead and with high code coverage.

In order to qualify the tools (modelling tools, compilers, static analysis, safety checker, etc.) according to ISO 26262, most manufacturers provide an ISO Kit greatly simplifying the necessary process. In this context, it is helpful to work with tools and manufacturers with a long track record in the automotive area. ISO 26262-8 uses the term 'proven in use' for this purpose: it is assumed that a tool that was frequently used over a long time with few problems will probably be less fault-prone than a new one.

Apart from addressing the safety risks outlined above, the compiler and its associated tools can help to mitigate the design risks associated with ADAS applications.

Dr. Herz concludes Part 2 of this article with a section on controlling design risks; click for pdf download.

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LEDLighting

HOW GAN IS TRANSFORMING RF ENERGY AND COOKING APPLICATIONS

By Mike Ziehl and Mark Murphy, MACOM

The RF energy market has evolved relatively slowly since magnetrons first came into widespread commercial use in microwave ovens in the early 1970s. Today, there exists a variety of use cases for RF energy, including industrial and consumer cooking, drying, lighting, medical, and automotive applications.

Recently, solid-state technology has appeared on the scene as a viable replacement and enhancement for magnetrons as the heating engine, delivering several key advantages: longer lifetime, enhanced reliability, precise power level and energy direction control, increased efficiency, and smaller dimensions.

Price and efficiency inhibiting growth

While the RF energy market is widely predicted to grow to as much as a billion dollars over the next five years, its expansion so far has been inhibited by solid-state technology limitations.

To reduce energy consumption requires high efficiency, less cooling or dissipated power heat sinking, which is an important consideration in all RF energy application designs. Ruggedness is critical for the harsh operating environments and unpredictable loads that the heating element is faced with during operation which, combined with the need for consistent power and long operating life, represents a huge disadvantage for existing magnetron technologies.

To date, the only solid state technology that has come close to the sector's tough cost targets has been silicon LDMOS. Driven by developments for basestations, LDMOS technology is well established with a competitive cost structure and volume supply chain. However, it falls short on efficiency (by more than 10%), ruggedness (due to lower breakdown voltage and lower operating temperature), and power density (which is only one-quarter to one-sixth of GaN).

GaN-on-SiC (gallium nitride on silicon carbide) can meet the necessary performance but has been unable to meet the necessary manufacturing scale and cost structure, and has traditionally been 5 to 10 times more expensive than legacy technologies – the physics of growing silicon carbide substrates is truly cost prohibitive even at large economies of scale.

However, as GaN transitions from traditional 4-inch compound semiconductor wafer fabs to 6-inch and 8-inch silicon fabs over the coming year, GaN-on-Si is starting to break through the cost threshold towards the ultimate goal set by the RF Energy Alliance of 5 cents per Watt, meaning that designers can finally move forward with mainstream deployment. For example, MACOM offers a 300W GaN-on-silicon device in plastic packaging that sells at around $15 and delivers over 70% efficiency. This level of price to performance has simply not been attainable until now.

RF energy in cooking applications

One of the largest potential RF energy markets today is found in RF cooking and heating applications. Well over 70 million microwave ovens are manufactured annually, spanning low-cost consumer grade to high-end professional and industrial ovens.

RF power transistors offer numerous performance advantages over traditional magnetrons, including better control of the cooking process through greater precision in setting the power level and RF energy direction inside the oven.

Today's microwave ovens lack effective control of the power level or the ability to direct the energy where required, which results in hot spots and over-cooking.

In the case of solid state devices, the frequency, amplitude, phase, pulse width and modulation can all be accurately controlled. With closed-loop control between the RF power amplifier and the RF synthesizer, a feedback loop enables the assessment of forward and reflected power levels, hence facilitating accurate and optimised control of

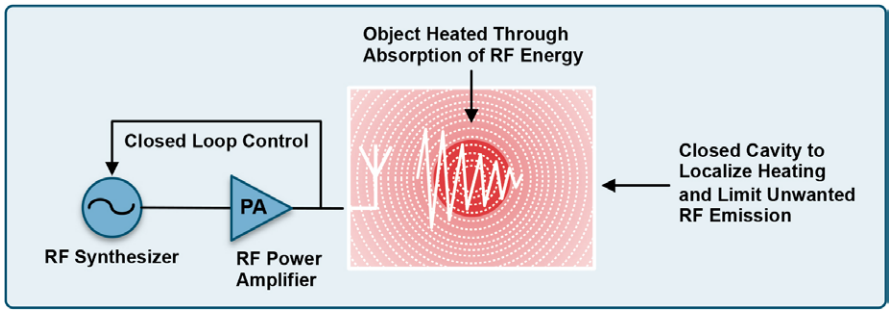


Figure 1. *Solid-state powered RF energy application*

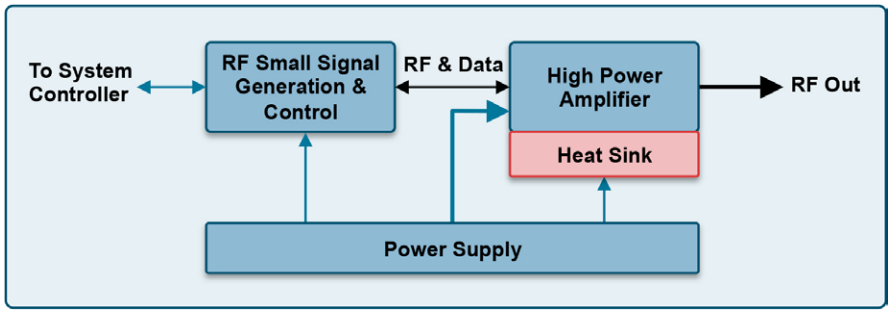


Figure 2. *Block diagram of a solid-state RF generator system*

the energy pattern.
This means that with three or four transistors and antennae, it is possible to direct the energy exactly to where it is required on the food, whilst the reflection and absorption of the radiation can be accurately measured. This feedback loop and the accurate control enabled by solid state transistors, enables an oven to accurately determine how well the food is cooked, and thus achieve reproducible results.

Varying the phase between multiple antennae can enable the field distribution inside the oven to be intelligently controlled to achieve homogeneous cooking results. Furthermore, by modifying the frequency and phase to match the food in the oven, very high RF energy delivery efficiency can be attained – above 90% even for small loads.
It has been demonstrated how a steak can be cooked on the same plate as ice cream without it melting, showing the precision of the directed RF energy. In practice, one gets outstanding control over internal meat temperature, with a tight tolerance of just one degree Celsius. Therefore, food can be cooked automatically, and one simply specifies the steak "doneness" level, for example, medium rare; and the oven will measure the food's properties and calculate the required settings.
Without having to manually enter the power levels, cooking is more predictable, and the interface more user-friendly.
As well as convenience, precise temperature control means that the cooked food is healthier and retains more of its nutrient content than is the case with traditional microwave ovens. The result is no more over-cooking or hotspots destroying nutrients and amino acid chains.

The solid state subsystem

For this kind of microwave oven application, a solid state RF generator subsystem could consist of the following:
- Small-signal generator, which may be co-located with a microcontroller
- High power amplifier connected to a heat sink
- Power supply

A block diagram for this system is shown above. The "RF Out" connection leads into an RF applicator, which may be a cavity or an otherwise confined environment. This contains the food absorbing the RF radiation and provides the required level of EMC shielding.

In the continuation of this article, the authors further explore issues of performance, reliability, lifetime and overall cost-competitiveness in moving to a GaN energy source. Click for pdf.

7 TIPS FOR OPTIMIZING EMBEDDED SOFTWARE

BY JACOB BENINGO

In an earlier column, I discussed key embedded system characteristics that in many cases require optimization. These characteristics include system timing, code size, RAM usage, and energy consumption. While optimizing each characteristic typically requires its own methods and techniques, there are several general tips developers can follow when optimizing their embedded software.

Tip No. 1 – Always create a baseline for comparison

Creating a baseline to compare optimization results against is obvious, and yet it would surprise you how many times I encounter teams in a hurry that jump straight into optimizing without any baseline. A baseline measurement is important because there are diminishing returns with each optimization cycle. For example, a first pass at optimizing for energy may result in a 20% improvement. The second, 10%, then 5%, and so on. Developers need to be able to see this trend and quantify the improvement they are seeing in the system as a function of their time input.

Tip No. 2 – Set an optimization target

Each optimization pass requires more and more time to squeeze just the smallest improvement from the system. Teams need to carefully balance their time investment and determine if the resultant improvement is worth the time. Simply trying to go as low as you can go can become addicting. Before one realizes it, one can be spending weeks optimizing a system that no longer needs to be optimized. Before optimization begins, then, teams should set a target level that -- once achieved -- is good enough for the current application. Achieving that target indicates that the optimization process has completed.

Tip No. 3 – Get the right tools to make measurements

Optimizing a system can be extremely difficult without the right measurements tools. Optimizing for energy, for instance, can't be done if there is not an accurate means to measure the system and microcontroller energy draws. In many cases I'll see teams fail to separate these two different energy measurements and attempt to minimize microcontroller energy when it can't go any lower.

Developers interested in optimizing for performance might find the Segger System View Utility, that I wrote about in Hands-on: Segger System View Utility, to be critical to understand which functions are monopolizing the CPU. Without tools that can accurately measure or allow a developer to peer into the system behaviour, there is no point in attempting to optimize a system.

Tip No. 4 – Use optimization tools

There are many areas of embedded software that can be optimized in order to decrease code size or improve performance. In some circumstances there are separate or add-on toolchains that can perform the optimizations. An example optimization tool is the Somnium DRT optimizer that can be used with GCC to optimize code size, energy usage, and performance.

Sometimes external tools may not be necessary, though. Just selection of the right toolchain may be sufficient. I recently wrote about Open Source versus Commercial Compilers where I explored the fact that in Coremark tests, under the same test conditions with the same microcontrollers, commercial compilers generated higher scores when compared with open source compilers such as GCC.

Tip No. 5 – Use compiler attributes and #pragma

In general, I strongly dislike using #pragmas or compiler attributes. Attributes and #pragmas are generally non-portable and changing compilers can result in software bugs. However, when it comes to fine tuning embedded software, developers will usually not have a choice. Using attributes and #pragma can improve speed, selectively apply

optimization to a single function, and so forth. So for those reasons, developers intent on optimizing software should get familiar with attributes, but also read Writing Portable Optimizations in C so that they can understand how to write optimizations that are still portable and won't come back to bite them.

Tip No. 6 – Don't hesitate to experiment

There is no set-in-stone practice for optimizing a system and developers shouldn't feel constrained to follow any specific technique. Sometimes the best way to learn and optimize a system is to put together experiments and just see what happens. When I first started optimizing systems for low power, there was a lot of trial and error associated with it. However, through experimentation and recording results, I was able to figure out what works, what doesn't, and what is a waste of resources and time. A simple example is given in how to Make the most of printf. Through trying different driver models there are ways to drastically improve the real-time performance a developer gets when using printf, which is usually assumed to be far better than it really is.

Tip No. 7 – Dig into the compiler-generated instructions

In applications that are extremely resource constrained, there comes a time when developers just need to roll up their sleeves and dig into the compiler-generated instructions. Selecting the

ternary operator over an if/else could potentially be the difference between three or four extra instructions being executed, which causes the application to implode. While languages such as C are standard, each compiler optimizes and generates the machine instructions slightly differently. The only real way to know what your compiler is doing is to review the assembly. (Check-out Ternary Operator versus if/else If you are interested in a low level look).

Conclusion

Applications will drastically vary on their optimization needs. Some applications that are in low volume production may require no optimization at all. In others, where every clock cycle or nano-amp matters, a vast amount of time may be spent trying to squeeze every last drop of performance or energy from the system. While each system is different, these tips provide developers and teams with a starting point that can get them on the road to a more efficient system.

Jacob Beningo *is an embedded software consultant who currently works with clients in more than a dozen countries to dramatically transform their businesses by improving product quality, cost and time to market. He has published more than 200 articles on embedded software development techniques, is a sought-after speaker and technical trainer and holds three degrees which include a Masters of Engineering from the University of Michigan. Feel free to contact him at jacob@beningo.com, at his website www.beningo.com, and sign-up for his monthly Embedded Bytes Newsletter here.*

LOW COST AND LOW DROP-OUT LINEAR AND SWITCHED-MODE SUPERCAP CHARGERS

By Dan Tooth, Texas Instruments

When the mains power fails, supercapacitors can provide back-up power to maintain system functionality for a period of time. The supercapacitor or "supercap" needs to be charged and how fast that charging should be is determined by the system requirements and leads to the choice of either a low current linear charger, or a switched-mode charger - should a fast re-charge time be required. This article looks at both types with an emphasis on both low drop-out, such as is the case when a 5V source is charging a 5.4V-rated supercap; and on low cost.

Supercap application

The application of interest is Smart e-Metering and has a high supercap discharge current, such as presented by a GSM/GPRS load, with an average load current of 500 mA being typical. This calls for a low ESR (equivalent series resistance) supercap and the device used for testing was a Cooper Bussmann PHV-5R4V255-R, which is a 5.4V(max), 2.5F, 75 mΩ device. The 5.4V rating applies at 65°C max and is linearly de-rated to 4V at 85°C. This supercap is a two-terminal device and will consist of two matched supercaps placed internally in series, to achieve the 5.4V rating.

Resistor charger

Figure 1 shows a simple supercap charger, which uses a resistor to charge the supercap. A TLV431 (or TL431) is present to clamp the voltage across the supercap to the desired level to prevent over-charging. Note that the clamp voltages of these devices when fully "on" are ~1V and ~2V respectively. The charge current is a maximum when the supercap is uncharged and decays exponentially towards zero as the supercap charges up towards the charging source voltage. The designer has to juggle the desired re-charge time (charge current) with the power dissipation in the resistor, which is at a maximum when the supercap is uncharged. The charge time is given by;

$$t = -RC \ln(1 - V_C/V_{DD})$$

where V_{DD} is the charging source voltage, V_C is the voltage across C, the supercapacitance, and R is the resistance through which it is being charged. The influence of the voltage divider across the supercap is ignored as it is a much larger resistance than the charging resistances.

For example, in Figure 1 then V_{DD} is a 5V charging source and the desired charge voltage across the supercap is set at 4V, which is the maximum value

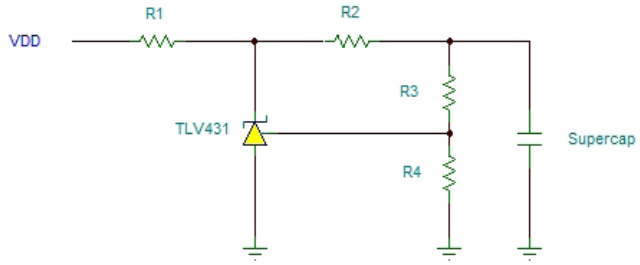


Figure 1. *Resistor charger with TLV431 overvoltage clamp*

for this Bussmann supercap at 85°C. If R1 = 110Ω and R2 = 25Ω then the initial charge current is 5V / 135Ω = 37 mA and the charge time is approximately 9 minutes. The charging resistance is split into R1 and R2 to provide some protection discharge resistance should the supercap discharge back through the TLV431. The TLV431 starts to conduct when its REF pin reaches 1.24V, which occurs at a supercap voltage of 4V given R3 = 6k and R4 = 2k7. When the supercap is fully charged, the TLV431 is shunting (5V – 4V) / 110Ω = 9 mA to GND.

Constant current source charger

To maintain the charging current constant throughout so as to charge the supercap faster, then another approach is to use a constant current source. The time taken to charge the supercap is

$t = C.V_C / I$

where I is the constant charging current. The reduced charging-time benefit of the constant current charger is not that significant if the source voltage V_{DD} and final capacitor voltage V_C are signigficantly different. For example, to charge a 2.5F supercap to 50% V_{DD} and keep the power dissipation in the charging resistor to 0.5W then a 50Ω resistor is used and the charge time is ~87 seconds. If a constant 100 mA current source is used instead, then the initial power dissipated is also 0.5W but the charging time is only reduced to be 62 seconds. If, on the other hand, the goal is to charge the supercap to 95% V_{DD}, then the charging resistor method will take more than 6 minutes, versus 2 minutes for the constant current source. The conclusion of this is that if the V_{DD} and desired V_C are similar, then a current source will charge the supercap much faster for the same peak power dissipation.

The technique used to achieve the current source here is to make use of an IC (TPS75100) that was designed to drive a constant current into LEDs. It has a low drop-out of ~100 mV at 15 mA, per channel. The IC is split into two banks of two current sources per bank (i.e. four current-source "channels" in total), each bank being controlled by its own enable pin. The constant current per channel is set by a programming resistor on the I_{SET} pin. Up to 25 mA can be sourced per channel and channels can be paralleled, to give up to a 100 mA current source if all four are paralleled together to drive a common load. TPS75100 (and TPS75105) are available in a QFN package with a power pad to dissipate the power. If the resistor on I_{SET} is unpopulated then the IC defaults to a fixed current per channel, which for TPS75100 is 10 mA and for TPS75105 is 5 mA. For an uncharged supercap, then the initial output voltage is 0V and the accuracy of the TPS75100 current source is worse, being ~12% tolerance, shown in Figure 12 of the datasheet and reaching specified tolerance (4% max) when the supercap voltage has risen to > 1.25V.

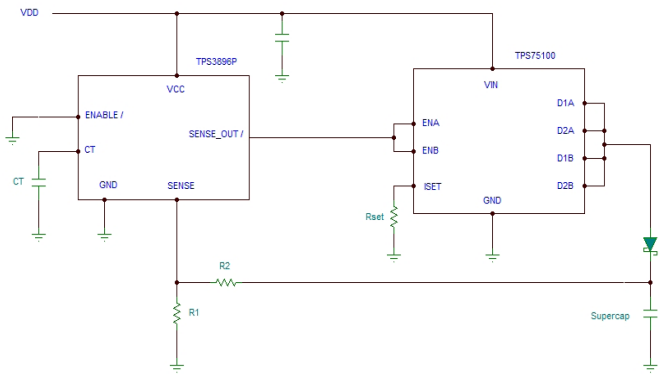


Figure 2. *TPS75100 charger, using TPS3896P as over voltage protection*

Figure 2 shows the implementation using TPS75100. TPS3896P is also used to regulate the desired voltage across the supercap. TPS3896P is only necessary should the input source voltage be greater than the max charge voltage of the supercap. TPS3896P is a voltage supervisor and when the voltage on its SENSE pin is ≥0.5V, it pulls its SENSE_OUT/ pin low for a delay time set by the capacitor on the CT pin. The delay provides a minimum on-time to prevent the TPS75100 being enabled/disabled too quickly.

For charging supercaps from a higher input voltage source then TPS7B7701-Q1 could be used. This has an accurate, programmable current limit and it also blocks reverse current flow. It is a linear regulator and the final charge voltage (output voltage) can easily be set. It also has various fault reporting features.

In the conclusion of this article, the author adds a switch-mode DC/DC charger to the options, and presents measured results from the circuits described – click for pdf.

AVOIDING THE ASIC VS FPGA GAMBLE; SMART ENGINEERING REQUIRES SMART SOC DESIGN

By Patrick Osterloh, Toshiba Electronics Europe

System on Chip (SoC) integration holds the key to delivering the smart and connected systems that are needed to manage life in the future, from autonomous driving to intelligent factories, and from advanced medical technology to consumer IoT devices. In many of these systems, an optimized SoC will be critical for delivering the advanced functionality, performance and connectivity required within tight size and power constraints – and at the right price.

Traditionally, designers have been presented with a choice of implementing their SoC as an ASIC, if the projected volumes have been high enough to amortise the relatively high design costs, or to use an FPGA if anticipated production volumes are lower. An FPGA can impose somewhat higher power consumption and greater cost per unit, in exchange for lower design costs and engineering risk.

Now, however, these relatively straightforward choices have become more complex. While on the one hand growing competition means it is tougher to achieve the large market share needed to justify high production volumes, the latest process nodes drive up the minimum volume at which an ASIC project becomes viable. Obvious project risks of an ASIC solution arise from the possibility that a product is not as successful as anticipated, or that logic changes would require an expensive re-spin.

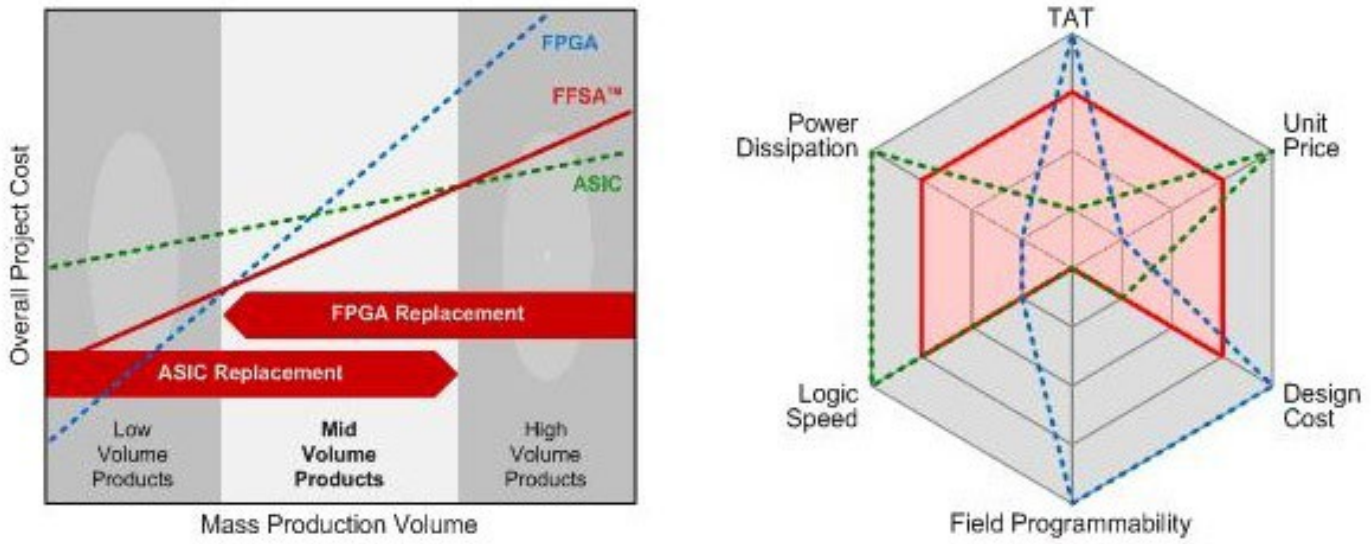
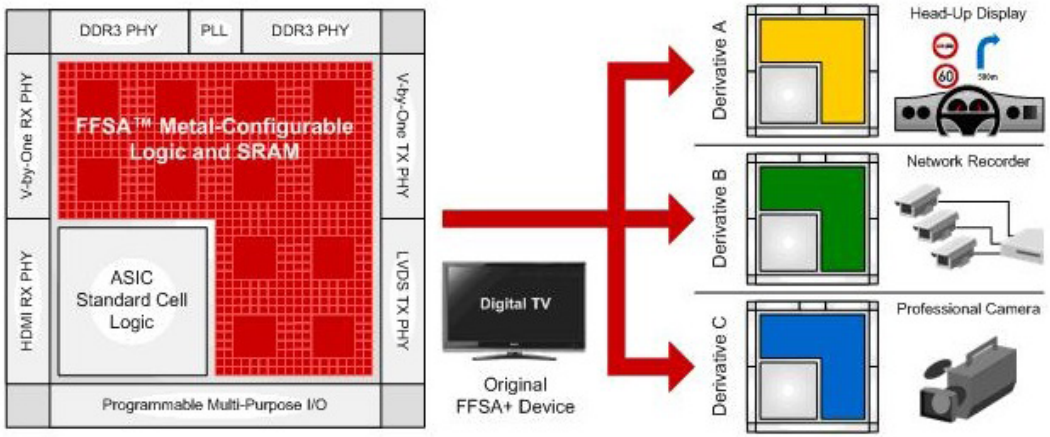


Figure 1. *FFSA, ASIC, FPGA comparison (red, green and blue profiles)*

Although the extra flexibility and faster turnaround time associated with an FPGA can deliver a critical first-to-market advantage, higher power consumption may result in battery life or product energy rating that is unacceptable to the market. Moreover, if the FPGA-based design becomes unexpectedly successful, the higher cost of each FPGA can significantly erode profits at high production volumes.

Despite the alternatives offered by established ASIC and FPGA vendors, such as structured ASICs, minimalist FPGAs or hard-copying services, the fact is that advancing CMOS technology nodes are exapnding the design gap between ASICs and FPGAs. It is increas-



Customizing a small number of layers cuts cost of creating product derivatives.

ingly difficult for designers of mid-volume custom SoC products to make the right decision for their projects when choosing between these two options. Effectively, designers are forced to place a bet on the success of their product.

Avoiding the gamble

There is now an alternative that can deliver ASIC-like computational performance, low power and reduced design cost, at affordable unit prices. Toshiba's Fit-Fast Structured Array (FFSA) technology fills the growing gap between ASICs and FPGAs, offering a supplementary design solution that can aid risk mitigation and cost management. Figure 1 compares FFSA with FPGA and ASIC design against key SoC project metrics.

This article continues by outlining the architecture and component parts of an FFSA, describing the available IP and the design process, and how the concept comprises an alternative technology and economic choice compared to the alternatives; click for full pdf.

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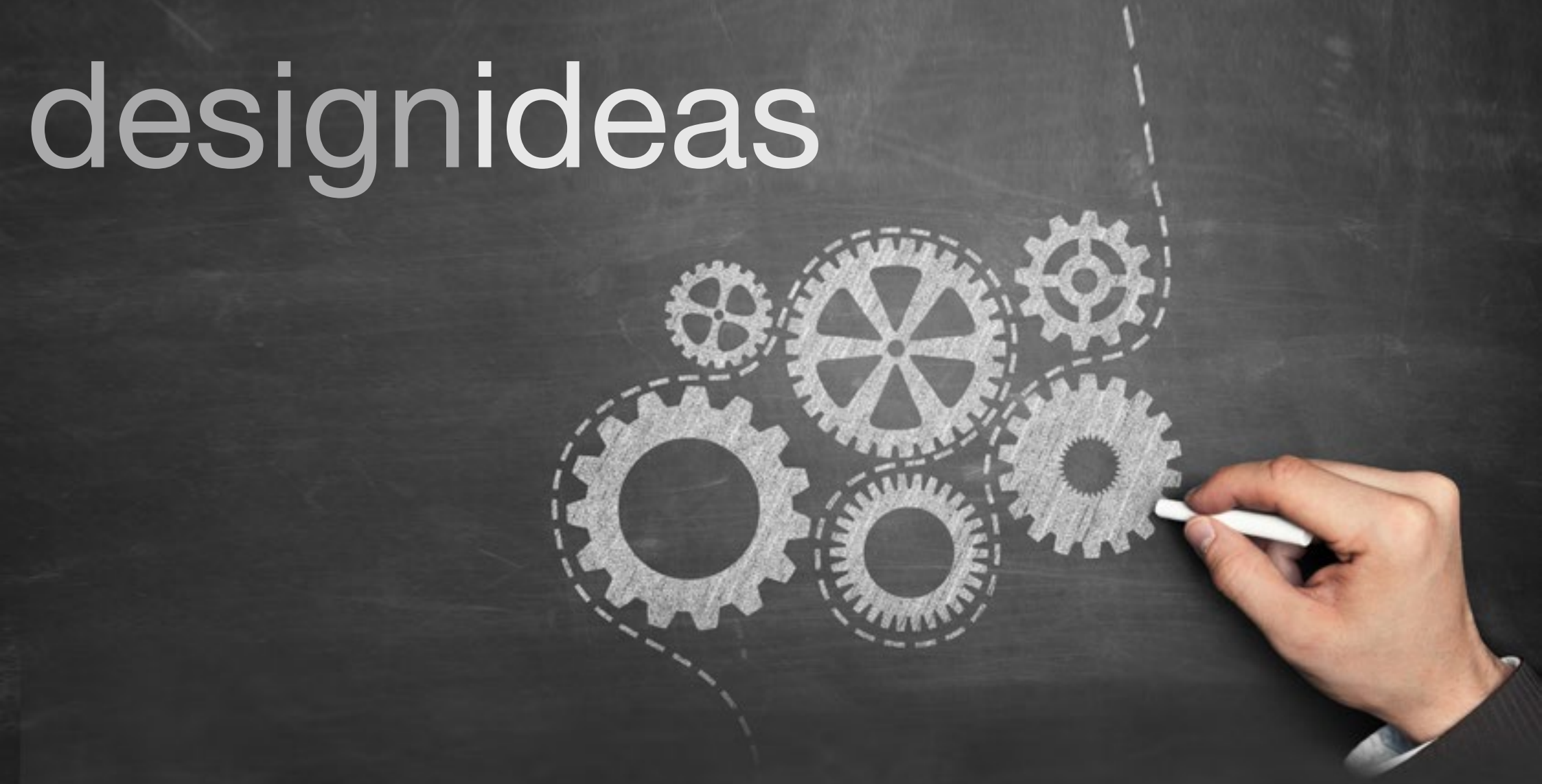


- LED strings driven by current source/mirror
- LTC Design Note: Electrolytic capacitor-based data backup power solution for a 12V system with 5V to 36V input

LED strings driven by current source/mirror

By Luca Bruno

The Design Idea in Figure 1 is a precision current mirror used to drive two strings of five white LEDs.

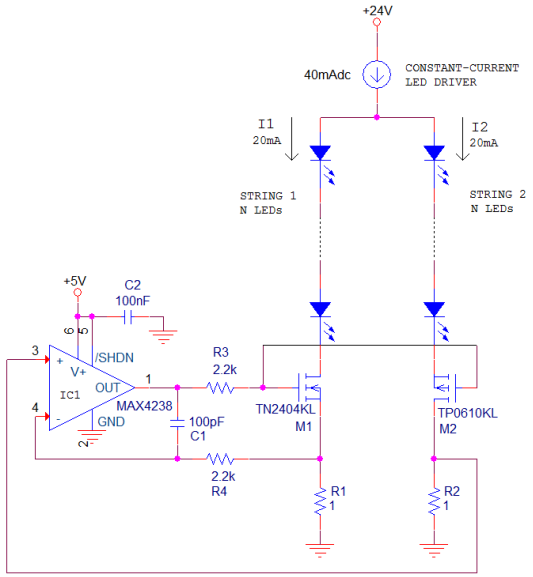


Figure 1.
Current source/mirror driving two LED strings

The op-amp has "double" negative feedback (since M2 inverts the signal at the non-inverting input). The voltage drops across R1 and R2 are equal, halving the LED driver current. MOSFET M2 works with a constant source-drain voltage (equal to the sum of $V_{GS1} + V_{GS2}$) while M1 absorbs the mismatch of the voltage drops of the two strings, even in the case where an LED is shorted.

To protect the LED string from overcurrent due to an open in one of the strings, you can add two diodes and one transistor as shown in Figure 2 and described in my previous Design Idea, Protect power-LED strings from overcurrent.

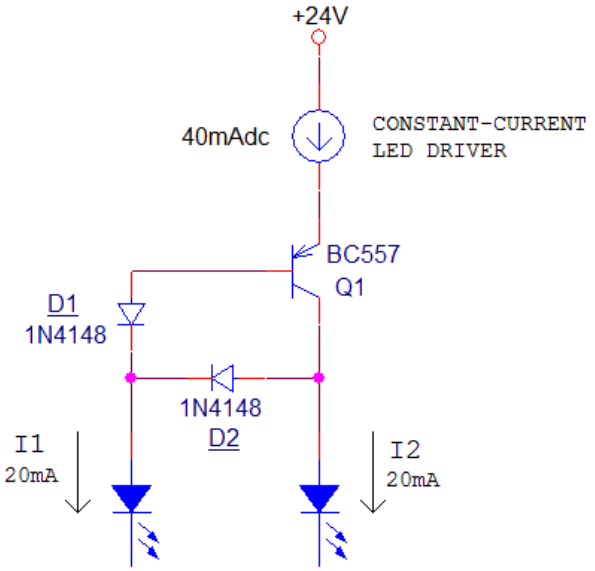


Figure 2.
Protection against opens

Capacitor C1 along with resistors R3 and R4 ensure stability of the op-amp. The voltage drop across R1 and R2 must be suitably greater than the maximum offset voltage of the op-amp to achieve good accuracy in dividing the LED driver current. The current ratio I1:I2 is equal only to the resistor ratio R1:R2.

The circuit is also suitable for driving power LEDs. In this case you should use MOSFETs with low threshold voltage to limit power dissipation, or you could replace them with a complementary pair of BJTs.

Luca Bruno *has a Masters Degree in Electronic Engineering from the Politecnico of Milan. He has written 16 EDN Design Ideas.*

LTC Design Note: Electrolytic capacitor-based data backup power solution for a 12V system with 5V to 36V input

By Victor Khasiev

Data loss is a concern in telecom, industrial and automotive applications where embedded systems depend on a consistent supply of power. Sudden power interruptions can corrupt data during read and write operations for hard drives and flash memory. Often, embedded systems need just 10 msec to 50 msec to backup volatile data to prevent loss.

Data backup is used in embedded systems for maintenance, troubleshooting and repair work. In complex industrial metal machining equipment, it's important to store the position and state of multiple tools after power disconnect to prevent equipment failure when power is later restored. These applications require a stable power supply and data retention, but unreliable power sources make it difficult to accomplish. Long supply lines, discharged batteries, unregulated AC adapters, load dumps, and switching high power electrical motors result in widely fallible input supplies. As a result, developers of embedded systems prefer to design with the widest possible input voltage range, enabling use in a variety of applications and environments.

Figure 1 shows a system that delivers reliable primary power plus holdup power for data backup. This solution is centred on the LTC3643 bidirectional power backup supply. When the input voltage is present, the LTC3643 charges the storage capacitor, $C_{STORAGE}$, up to 40V in boost mode. When the input voltage is interrupted, the LTC3643 discharges the storage capacitor into the load in buck mode, keeping the nominal voltage at the load (V_{SYS}) in the range of 3V to 17V.

The relatively high voltage of the backup storage rail increases stored energy of this solution ($E = CV^2/2$) and enables the use of electrolytic capacitors as a backup storage component. Electrolytic capacitors are inexpensive and widely available, significantly reducing the cost of the backup solution. Another advantage of the LTC3643 is its ability to support 12V systems, the default standard voltage rail in many automotive and industrial applications.

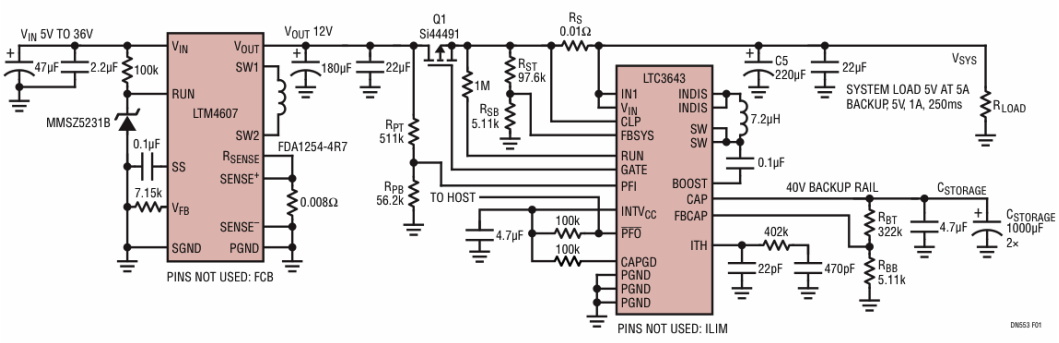


Figure 1. *LTC3643 backup supply*

In Figure 1, the LTM4607 µModule (micromodule) buck-boost converter acts as the front end regulator, producing 12V at up to 5A from a 5V to 36V input, such as a vehicle battery. The buck-boost regulator maintains a steady 12V output so long as the input voltage stays within the specified range, allowing V_{SYS} to ride through brownout and overvoltage conditions such as automotive cold crank and load dump. When the input voltage is interrupted or moves out of this range, the LTC3643

based backup power solution maintains the V_{SYS} system voltage to allow for short-term data backup.

Circuit functionality

In normal operation, when the P-channel MOSFET Q1 is on, the flag PFO is low and the electrolytic capacitor array $C_{STORAGE}$ is charged to 40V. When the input voltage is interrupted, the LTC3643 turns Q1 off, sets the flag PFO high and starts to discharge the $C_{STORAGE}$ capacitor array, maintaining 12V to the load. When Q1 is in the off state, the body diode of this transistor effectively isolates the load from the input lines. The PFO flag identifies the fault and signals the host computer to disconnect the non-critical loads and supply circuitry. Here it is assumed that the critical circuitry related to data retention consumes 1A for up to 100 msec.

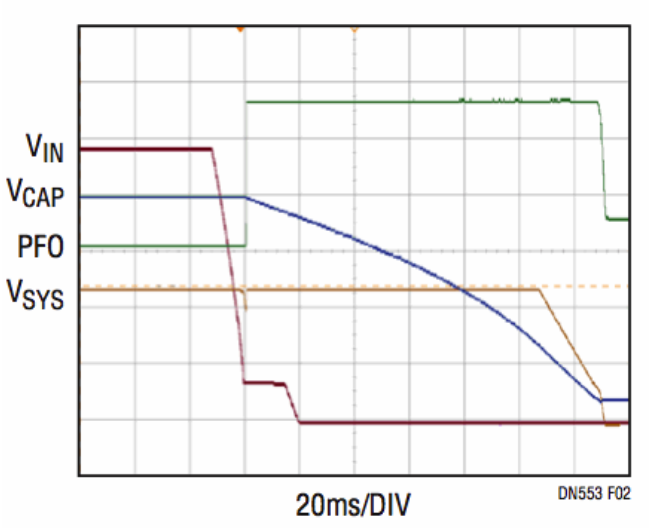


Figure 2. *Switchover waveforms, V_{SYS} = Load voltage, V_{IN} = Input voltage, PFO = Flag status, V_{CAP} = $C_{STORAGE}$ voltage (V_{SYS} and V_{IN} = 5V/div, V_{CAP} = 10V/div, PFO 1V/div)*

Figure 2 illustrates the entire switchover process. At the start, the system load is supplied by the LTM4607, as the input voltage is present. When the input voltage is interrupted, the LTC3643 supports the system load by discharging the storage capacitor. Figure 3 shows the timing of the switchover in more detail. The load voltage falls to 10V, a value set by the resistor divider R_{PT}/R_{PB} and then recovers to the nominal 12V, set by the resistor divider R_{ST}/R_{SB}.

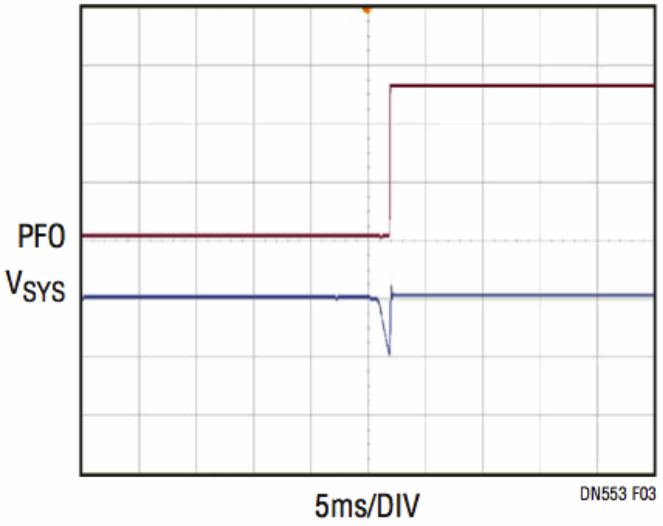


Figure 3. *Detailed view of switching waveforms (PFO 1V/div, V_{SYS} 2V/div)*

The formulas for an estimation of the required storage capacitance and holdup time are below. If a more detailed analysis is needed, the necessary information can be found in vendor's documentation.

1. Energy Stored

$$E_{CAP} = \frac{C_{STORAGE}}{2} \bullet (V_{CAP}^2 - V_{SYS}^2)$$

2. Energy Needed to Supply Load for Time T_H

$$E_{LOAD} = I_{SYS} \bullet V_{SYS} \bullet T_H$$

3. Holdup Time

$$T_H = \frac{C_{STORAGE} \bullet \left(V_{CAP}^2 - V_{SYS}^2\right) \bullet \eta}{2 \bullet I_{SYS} \bullet V_{SYS}}$$

η = efficiency

4. Storage Capacitance

$$C_{STORAGE} = \frac{2 \bullet V_{SYS} \bullet I_{SYS} \bullet T_H}{V_{CAP}^2 - V_{SYS}^2}$$

The LTC3643 is a highly integrated, high performance backup regulator. The design shown in this Design Note combines the advantages of this IC with a high efficiency buck-boost LTM4607 µModule regulator. Together, these devices enable a small footprint, efficient and cost effective solution for data retention and backup in automotive and industrial applications.

(Download this Linear Technology Design Note as a pdf.)

productroundup

productroundup

AEC-Q100-Qualified 8-bit MCUs for motor control

Silicon Labs has introduced two families of automotive-grade EFM8 microcontrollers designed to handle in-cabin touch interface and body electronics motor control applications. TheAEC-Q100-qualified, ultra-low-power EFM8SB1 Sleepy Bee family provides on-chip capacitive touch technology enabling replacement of physical buttons with touch control. All EFM8 MCUs are 8-bit devices based on a high-speed pipelined 8051 core, ultra-low power, precision analogue and enhanced communication peripherals, on-chip oscillators, and a crossbar I/O pin routing architecture.

Complete article, here

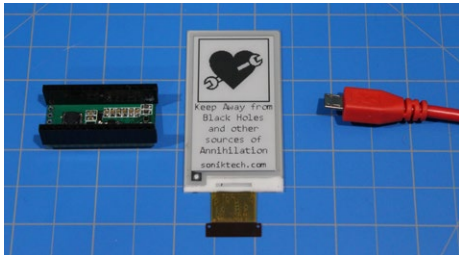
Sub-1-GHz, ultra-low-power ISM-band RF transceiver

Maxim Integrated has posted initial details of a quad-band transceiver, that includes an 8051 processor core, for low-power, battery-operated applications such as (automotive) remote keyless entry and tyre pressure monitoring; smart-home devices and building automation; smart meters; and ultra-low-power sensor networks. The MAX7037 has, in addition to the quad band multichannel transceiver and integrated microcontroller, flash memory, and a sensor interface. It runs from a minimum supply voltage of 2.1V, extending battery life and also enabling it to make use of harvested energy. Hardware-implemented transmit-and-receive routines in combination with a microcontroller enable a high-efficiency transceiver system for wireless fail-safe multiband/multichannel communication with advanced FSK and ASK protocol features.

Complete article, here

e-paper experimenter/starter kit with simple MCU board

Pervasive Displays (Pdi) (Tainan City, Taiwan) has configured an e-paper shield starter kit to help makers and hobbyists integrate e-paper into any project needing a display. The kit, which is open-sourced and based around the Teensy LC microcontroller board, was created by SonikTech and is a starting point for makers trying out an inexpensive, low power e-paper display in their design. E-paper displays do not require a power source to maintain an image and give crisp, detailed text and images. Displays are fully readable in sunlight with no backlighting needed.



Complete article, here

Arduino-compatible shield for stepper driver designs

Rohm Semiconductor has designed an Arduino-based evaluation kit (EVK) to support the evaluation of its motor driver devices: the shield plugs directly into the Arduino main board, and the EVK integrates a Rohm's HTSSOP-B28 packaged stepper motor drive IC allowing engineers to rapidly prototype their stepper motor systems. The EVK comes in 15 different variants for Rohm's stepper motor driver ICs– from standard, micro step, low voltage to high voltage. The solution covers supply voltages from 8V to 42V, enables up to 2.5A per phase, as well as micro-stepping and single- or multi-phase control.

Complete article, here

productroundup

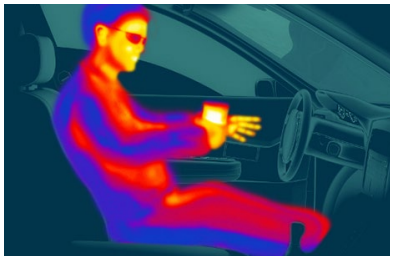
RISC-V SoC analysis and debug, from Codasip & UltraSoC

Codasip (San Jose, California), provider of IP to fabricate processor cores in the RISC-V architecture; and UltraSoC (Cambridge, UK) provider of semiconductor IP for on-chip analytics, performance optimization and hardware-based security and debug, have announced a collaboration to integrate the Codix-Bk series of RISC-V compliant processor cores seamlessly with the UltraSoC environment. While RISC-V provides an ISA for processor IP, it does not in itself solve all the other problems of support, commercialization or development. This partnership aims to serve that need; Codasip provides proven processor IP and infrastructure, while UltraSoC extends this to enable a rich and versatile toolkit for debug, optimization and analytics.

Complete article, here

Infra-red sensor array offers low-res thermal imaging/detection

Melexis (Tessenderlo, Belgium) recently announced its MLX90640 infrared (IR) sensor array that offers a cost-effective alternative to more expensive high-end thermal cameras. It can provide advanced detection features where there is no requirement for detailed imaging. The resolution is sufficient to detect, and thermally map, the presence of a person or persons in its field of view; but can be intentionally configured to be less than would be required to identify them. The sensor has a -40°C to 85°C operational temperature range and can measure object temperatures between -40°C and 300°C.



Complete article, here

16-bit current measuring module for automotive, industrial

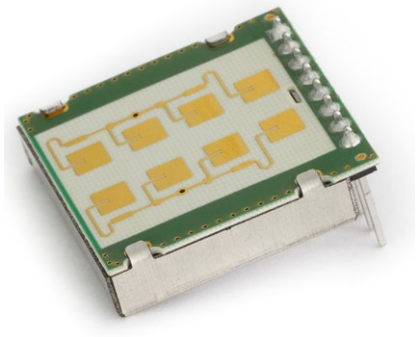
ICD-A is an automotive measuring technology system from Isabellenhütte, designed for use in restricted spaces. It combines a current measurement shunt and 16-bit A/D conversion, outputting data on CAN bus via a sealed six-pole MCON connector. With transmission rates of up to 1 Mbit/sec, the connection provides digitised data in CAN bus 2.0 format.

The ICD-A is available in three variations with different current levels: 100A, 300A and 500A. Alongside the automotive solution, Isabellenhütte also offers a version of the measurement technology system for industry in the form of the ICD-C model.

Complete article, here

24 GHz radar module minimises size & power

Presented as the smallest and lowest-power single transceiver available, this module by RFbeam Microwave employs low-cost 24 GHz industrial radar chips from Infineon. Infineon and RFbeam Microwave (St. Gallen, Switzerland) have collaborated to produce the single Tx/Rx module; low-cost 24 GHz transceiver system modules from RFbeam use Infineon BGT24LTR11 and BGT24MR2 24 GHz radar sensors. They provide a plug-and-play-solution for original equipment manufacturers in need of either motion detection for persons or speed/distance measurement capabilities.



Complete article, here

productroundup

5in. format Arduino-compatible touch-display shield

Bridgetek and FTDI are expanding their CleO smart display product family to include a higher end version. Based on the Embedded Video Engine (EVE) technology, the CleO50 shield has a larger 5.0 in. diagonal 800x480 pixel resolution TFT with built-in resistive touch screen, plus enhanced audio capabilities. It incorporates an FT900 low power, performance-optimised 32-bit microcontroller with 8MBytes of on-board Flash memory and FT812 EVE graphics controller to support the larger, higher resolution screen with 24-bit colour depth and video playback capabilities.

Complete article, here

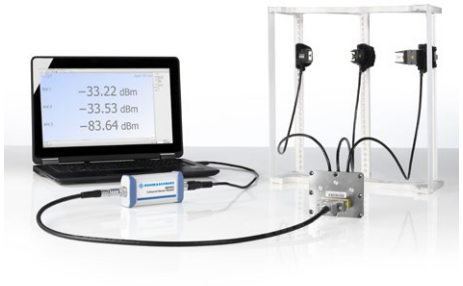
Cypress/Broadcom IoT multi-protocol wireless development

Cypress Semiconductor has announced a new version of its development platform for the Internet of Things (IoT) that enables wireless connectivity in minutes. The Wireless Internet Connectivity for Embedded Devices (WICED) Studio 4 platform provides a single development environment for multiple wireless technologies, including Cypress's Wi-Fi, Bluetooth and combo solutions, with an application programming interface. The WICED platform supports the most popular cloud services and removes the need for developers to implement the various protocols to connect to them.

Complete article, here

Over-the-air power measurement to 75 GHz

Rohde & Schwarz' NRPM OTA power measurement solution is presented as the first solution for measuring transmit power over the air interface for 5G and wireless gigabit components, to calibrate the output power of the antenna on a DUT and to test the DUT's beamforming function. The solution works in the frequency range from 27.5 GHz to 75 GHz and therefore covers the 28 GHz band currently being discussed for 5G as well as the frequency range from 55 GHz to 66 GHz for WLAN in line with IEEE 802.11ad and frequencies above 66 GHz in line with IEEE 802.11ay.



Complete article, here

Hi-resolution and -voltage, 14-bit PXI oscilloscope

National Instruments (NI) has announced a high-speed, high-resolution, high-voltage oscilloscope in the PXI card format, that offers 100 Vpp maximum input range at 1 Gsample/sec and 14 bits. The PXIe-5164 is built on the open, modular PXI architecture, and includes a user-programmable FPGA to help aerospace/defence, semiconductor and research/physics applications that require high-voltage measurements and high levels of amplitude accuracy. The PXIe-5164 features two 14-bit channels sampled at 1 Gsample/sec with 400 MHz bandwidth and two Category II-rated channels with voltage input range to 100 Vpp.

Complete article, here

productroundup

ST bases intelligent motion-control SiP on STM32

Aiming it at "smart industry and high-end consumer", STMicroelectronics has configured an integrated system-in-package (SiP) that simplifies intelligent motor control for smart-manufacturing equipment, drones, high-performance home appliances, and portable BLDC motors. The STM32 microcontroller-based development environment includes tools and software, which includes motor-control algorithms. The STSPIN32F0 combines a microcontroller and an analogue IC in a 7 x 7 mm QFN package, delivering the flexibility and power of a microcontroller-based motor drive with the convenience, simplicity, and space-efficiency of a single IC.

Complete article, here

Intel Joule IoT apps development platform, in distribution

Distributor RS Components has the Intel Joule compute modules and development kits that target developers, inventors, and OEMs for Internet of Things applications, enabling rapid prototyping. The Intel Joule 550x compute module features a 64-bit 1.5 GHz quad-core Intel Atom processor T5500, plus 3 GB LPDDR4 RAM and 8 GB eMMC memory. The higher-performance Intel Joule 570x compute module features a 64-bit 1.7 GHz quad-core Intel Atom processor T5700 with Intel Burst Technology allowing operation at 2.4 GHz, plus 4 GB LPDDR4 RAM and 16 GB eMMC memory.

Complete article, here

Prototype 'mid-air touch' controls with Ultrahaptics' dev kit

Simplifying evaluation and prototyping of mid-air haptics in touchless gesture controls, Ultrahaptics (Bristol, UK) has introduced a development platform that allows companies looking to evolve innovative control solutions a route to easily evaluate and appreciate the benefits of gesture controls enhanced by tactile feedback sensations. The UHDK5 TOUCH Development Kit provides a complete hardware and software package with an architecture that can readily be embedded in product designs, from prototypes right through to volume production.

Complete article, here

Ultra-small hSensor platform for wearable wellness apps

For wearable products in the health and fitness applications space, Maxim has configured a complete development platform that uses ARM mbed support. Maxim says its hSensor Platform eliminates the extra 3-6 months it typically takes to develop a prototype by bringing all the hardware building blocks together on one PCB, as well as having readily-accessible hardware functionality with the ARM mbed hardware development kit (HDK). The hSensor Platform, offered as the MAXREFDES100# reference design, includes an hSensor board, complete firmware with drivers, a debugger board, and a graphical user interface (GUI). The hSensor Platform spans health, wellness, and high-end fitness applications such as chest straps, ECG patches, wrist-worn devices, thermometers, disposable temperature patches, blood oxygen measurement, smart weigh scales, and bio authentication.

Complete article, here

BY MICHAEL KORNACKER

The chip glitch

In the manufacturing department of this defence company, we build what is commonly referred to as a black box for our military. In the black box are circuit cards of various functions plugged into a motherboard.

One day, a software engineer was tasked to investigate and troubleshoot why six circuit cards of the same type were failing in the box. The cards had been sitting in a "bone pile" for quite a while because no one could figure out what was the matter with them. Each circuit card was worth about $10,000 and management didn't want to scrap them if at all possible. Apparently they were passing test on the test fixture but they just would not work correctly in the box.

The software engineer who had been working on them for a couple of days came to me to ask my advice on troubleshooting them since, before I became an engineer, I was the technician who tested these cards. I told him I'd help, but I knew trying to troubleshoot these cards in the box would be very difficult. This card had about 30 discrete chips in the failing circuit and probing it for the bad signal was not going to be easy. However, if we could fix one, then we'd have all six cards fixed, since they were failing the same way. He then told me that, when he writes to certain registers on the card, he can get it to fail at will. Excellent, I thought. He's done quite a bit of troubleshooting already. This might be easier than I thought.

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I told him we shouldn't use the box to troubleshoot it, but since he discovered how to easily get it to fail, then we should be able to look at it on the test fixture, which should make it easier to analyze it. I put the card on the test fixture, set it up, and discovered quite quickly what the problem was. The problem was that somehow the circuit was getting an inadvertent reset command. I got my scope out and started probing around. It didn't take but a few minutes to discover the cause.

The circuit employed a quad 2 to 1 mux chip 54ALS157. Two inputs to one output switched by an input control logic. I discovered that when the switch input control logic was changed on one of the sections it generated a 10 nsec glitch on the output line and that this output line was connected to the reset circuitry.

In other words, there was something wrong with the chip. It should not generate a glitch when the switch was toggled one way or the other. We checked all six cards with the scope and they all exhibited the same glitch. We visually looked at all six circuit cards and found that they all had the same date code on the chip. Apparently, the chips were from a bad lot from the manufacturer. Just one of those things that occasionally happens. Having the chips replaced should fix the cards. After the repair, the six circuit cards finally passed both on the test fixture and in the box. We saved $60k and management was happy. The software engineer and I both got a nice monetary reward.

Mike Kornacker has been an electrical engineer in the defence industry for over 30 years.

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